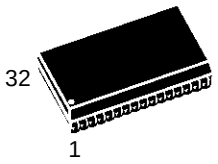
SGS-THOMSON MICROELECTRONICS

M638128

LOW VOLTAGE 1 Megabit (128K x 8) VERY FAST SRAM WITH OUTPUT ENABLE

DATA BRIEFING

- LOW VOLTAGE: 3.3V ± 0.3V
- 128K x 8 VERY FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE

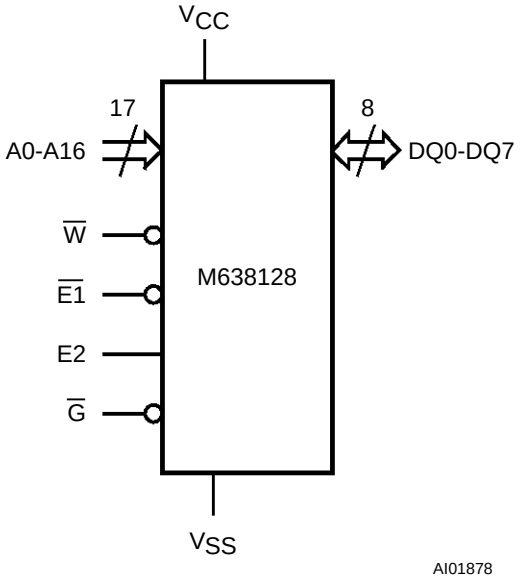


SOJ32 (E)
300 mils

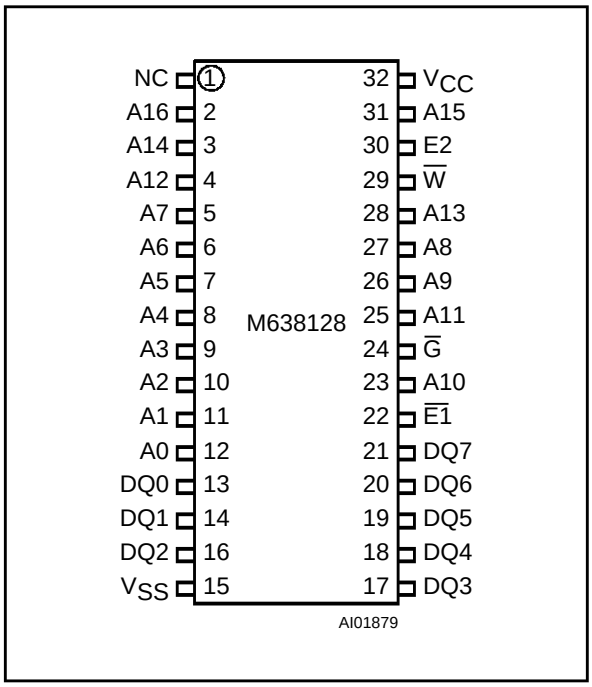
DESCRIPTION

The M638128 is a 1 Megabit (1,048,576 bit) Fast CMOS SRAM, organized as 131,072 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 3.3V ± 0.3V supply, and all inputs and outputs are TTL compatible.

Logic Diagram



SOJ Pin Connections



Warning: NC = Not Connected.

Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: M638128 -15 E 1

Speed

-12 12ns
-15 15ns
-20 20ns

Package

E SOJ32 300 mils

Temp. Range

1 0 to 70 °C