

74VHC02 Quad 2-Input NOR Gate

General Description

The 74VHC02 is an advanced high-speed CMOS 2-Input NOR Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back-up. This circuit prevents device destruction due to mismatched supply and input voltages.

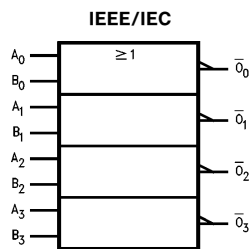
Features

- Low power dissipation:
 $I_{CC} = 2 \mu\text{A}$ (max) at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Low noise: $V_{OLP} = 0.8\text{V}$ (max)
- Pin and function compatible with 74HC02

Commercial	Package Number	Package Description
74VHC02M	M14A	14-Lead Molded JEDEC SOIC
74VHC02SJ	M14D	14-Lead Molded EIAJ SOIC
74VHC02MSC	MSC14	14-Lead Molded EIAJ Type 1 SSOP
74VHC02MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC02N	N14A	14-Lead Molded DIP

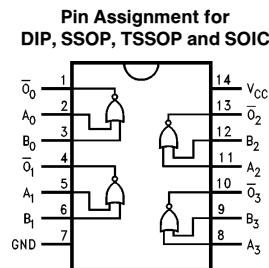
Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
EIAJ Type 1 SSOP available on tape and reel only, order MSCX.

Logic Symbol



TL/F/11515-1

Connection Diagram



TL/F/11515-2

Truth Table

A	B	O
L	L	H
L	H	L
H	L	L
H	H	L

Pin Description

Pin Names	Description
An, Bn	Inputs
On	Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	-20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC} /GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC				Units	Conditions	
			$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			
			Min	Typ	Max	Min			Max
V_{IH}	High Level Input Voltage	2.0 3.0-5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}	V		
V_{IL}	Low Level Input Voltage	2.0 3.0-5.5		0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu\text{A}$	
		3.0 4.5	2.58 3.94			2.48 3.80	V	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1	0.1	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$	
		3.0 4.5		0.36 0.36		0.44 0.44	V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	
I_{IN}	Input Leakage Current	0-5.5		±0.1		±1.0	μA	$V_{IN} = 5.5\text{V}$ or GND	
I_{CC}	Quiescent Supply Current	5.5		2.0		20.0	μA	$V_{IN} = V_{CC}$ or GND	

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC		Units	Conditions
			T _A = 25°C			
			Typ	Limits		
V _{OLP} *	Quiet Output Maximum Dynamic V _{OL}	5.0	0.3	0.8	V	C _L = 50 pF
V _{OLV} *	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.3	-0.8	V	C _L = 50 pF
V _{IHD} *	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF
V _{ILD} *	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF

*Parameter guaranteed by design.

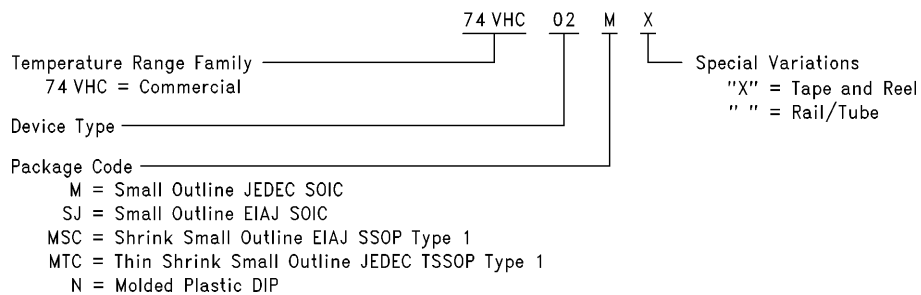
AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	74VHC				Units	Conditions	
			T _A = 25°C			T _A = -40°C to +85°C			
			Min	Typ	Max	Min			Max
t _{PHL} , t _{PLH}	Propagation Delay	3.3 ± 0.3	5.6	7.9	1.0	9.5	ns	C _L = 15 pF	
			8.1	11.4	1.0	13.0		C _L = 50 pF	
		5.0 ± 0.5	3.6	5.5	1.0	6.5	ns	C _L = 15 pF	
			5.1	7.5	1.0	8.5		C _L = 50 pF	
C _{IN}	Input Capacitance		4	10	10	pF	V _{CC} = Open		
C _{PD}	Power Dissipation Capacitance		15			pF	(Note 1)		

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate).

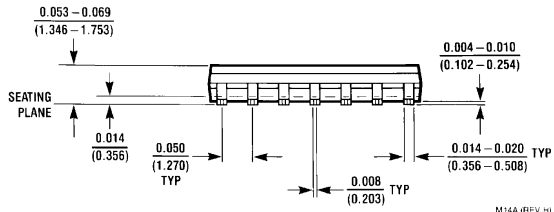
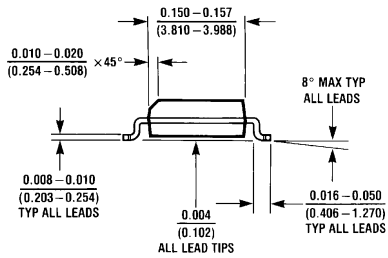
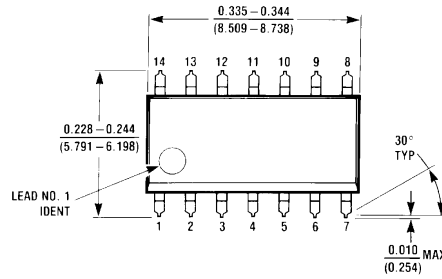
Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



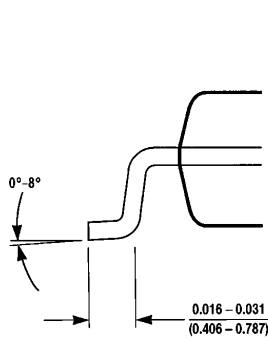
TL/F/11515-3

Physical Dimensions inches (millimeters)

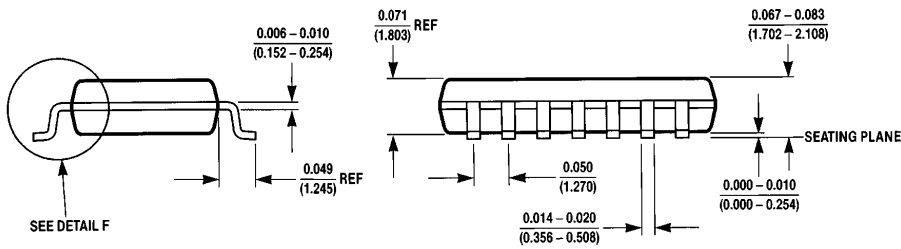
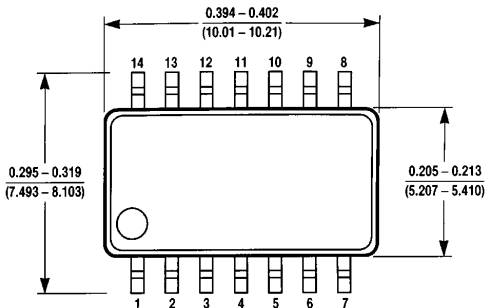


M14A (REV H)

**14-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
NS Package Number M14A**



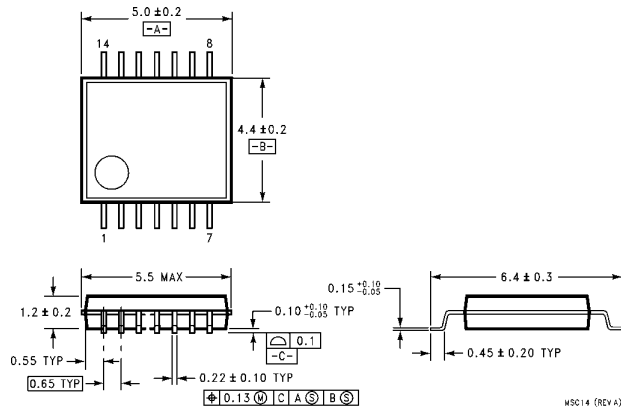
DETAIL F



M14D (REV A)

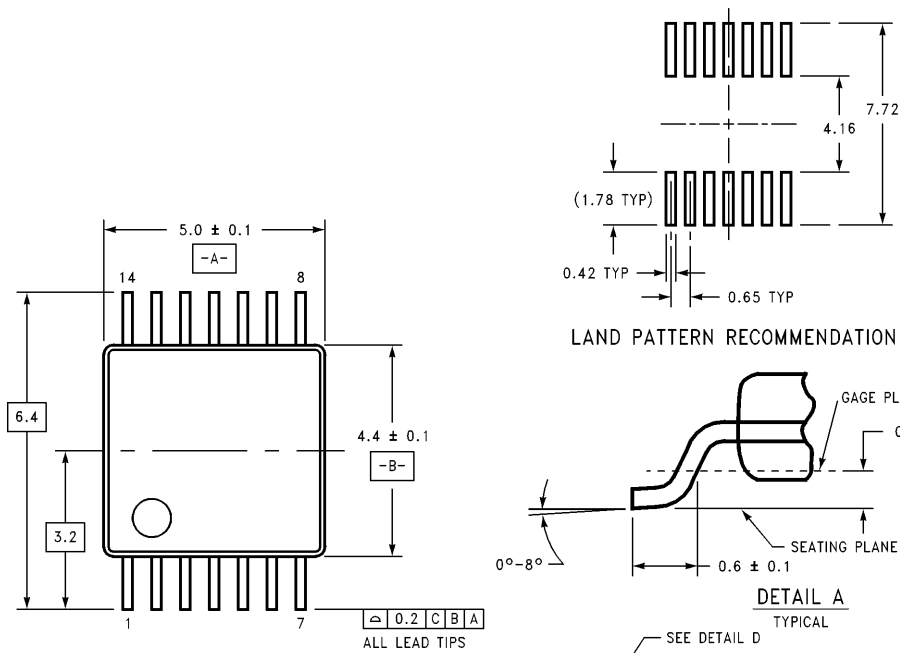
**14-Lead Plastic EIAJ SOIC (SJ)
NS Package Number M14D**

Physical Dimensions inches (millimeters) (Continued)



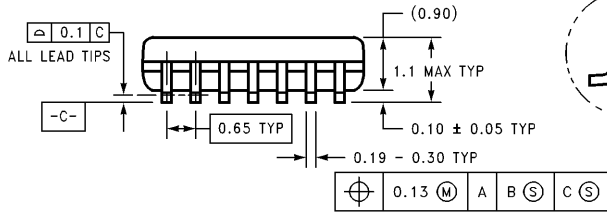
14-Lead Plastic EIAJ SSOP Type 1 (MSC)
NS Package Number MSC14

MSC14 (REV A)



LAND PATTERN RECOMMENDATION

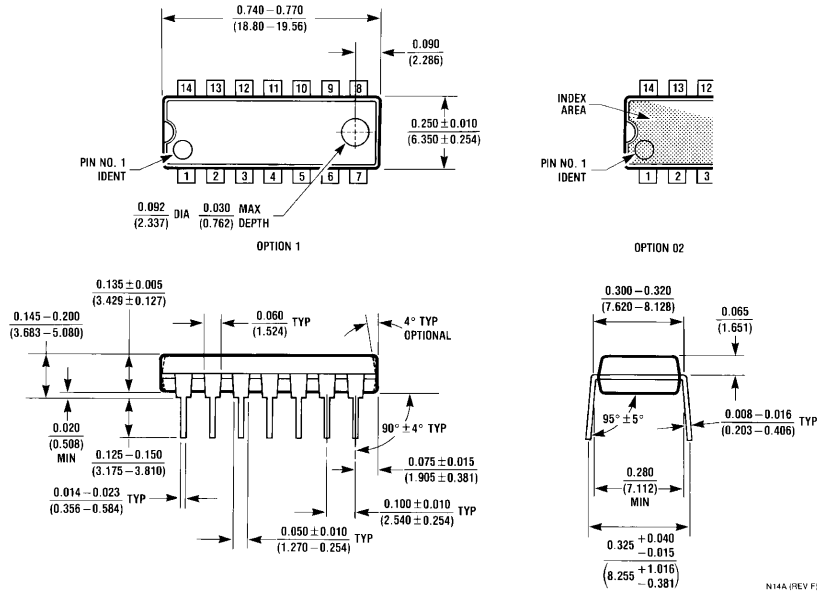
DETAIL A
TYPICAL



14-Lead Molded JEDEC Type I TSSOP
NS Package Number MTC14

MTC14 (REV B)

Physical Dimensions inches (millimeters) (Continued)



**14-Lead (0.300" Wide) Molded Dual-In-Line Package
NS Package Number N14A**

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