National Semiconductor

October 1995

74LVXC4245
8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

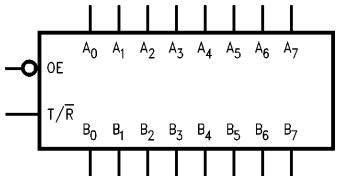
General Description

The LVXC4245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 5V supply level. The "A" port is a dedicated 5V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The "B" port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. This device will allow the V_{CCB} voltage source pin and I/O pins on the "B" port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 5V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 74 series 245

Logic Symbol



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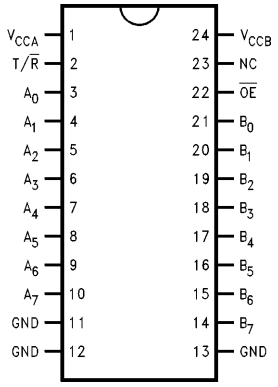
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



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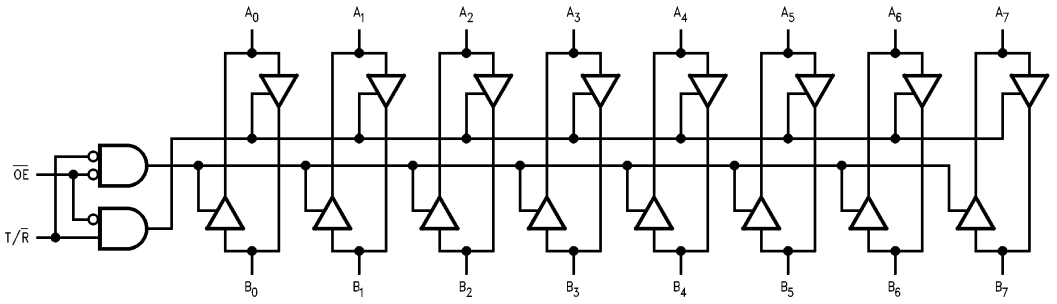
	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVXC4245WM 74LVXC4245WMX	74LVXC4245QSC 74LVXC4245QSCX	74LVXC4245MTC 74LVXC4245MTCX
See NS Package Number	M24B	MQA24	MTC24

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA},V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} +0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	−0.5V to V_{CCA} +0.5V
@ B_n	−0.5V to V_{CCB} +0.5V
DC Input Diode Current (I_{IK}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
Per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current	±200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions

Supply Voltage V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@A_n	0V to V_{CCA}
@B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3V, 4.5V, 5.5V	

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC4245			Units	Conditions
					T_A = +25°C	T_A = −40°C to +85°C			
					Typ	Guaranteed Limits			
V_{IHA}	Minimum High Level Input Voltage	A_n	4.5	2.7		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6		2.0	2.0		
		T/$\overline{R}$	5.5	5.5		2.0	2.0		
V_{IHB}		B_n	4.5	2.7		2.0	2.0		
			4.5	3.6		2.0	2.0		
			4.5	5.5		3.85	3.85		
V_{ILA}	Maximum Low Level Input Voltage	A_n	4.5	2.7		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		$\overline{OE}$	4.5	3.6		0.8	0.8		
		T/$\overline{R}$	5.5	5.5		0.8	0.8		
V_{ILB}		B_n	4.5	2.7		0.8	0.8		
			4.5	3.6		0.8	0.8		
			4.5	5.5		1.65	1.65		
V_{OHA}	Minimum High Level Output Voltage		4.5	3.0	4.49	4.4	4.4	V	$I_{OUT} = -100\ \mu A$
			4.5	3.0	4.25	3.86	3.76		$I_{OH} = -24$ mA
V_{OHB}			4.5	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100\ \mu A$
			4.5	3.0	2.85	2.56	2.46		$I_{OH} = -12$ mA
			4.5	3.0	2.65	2.35	2.25		$I_{OH} = -24$ mA
			4.5	2.7	2.5	2.3	2.2		$I_{OH} = -12$ mA
			4.5	2.7	2.3	2.1	2.0		$I_{OH} = -24$ mA
			4.5	4.5	4.25	3.86	3.76		$I_{OH} = -24$ mA
V_{OLA}	Maximum Low Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			4.5	3.0	0.21	0.36	0.44		$I_{OL} = 24$ mA
V_{OLB}			4.5	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100\ \mu A$
			4.5	3.0	0.21	0.36	0.44		$I_{OL} = 24$ mA
			4.5	2.7	0.11	0.36	0.44		$I_{OL} = 12$ mA
			4.5	2.7	0.22	0.42	0.5		$I_{OL} = 24$ mA
			4.5	4.5	0.18	0.36	0.44		$I_{OL} = 24$ mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	74LVXC4245			Units	Conditions
					$T_A = +25°C$	$T_A = -40°C$ to $+85°C$			
					Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		5.5 5.5	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA	$V_I = V_{CCA}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A_n		5.5 5.5	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}$, V_{IH}, $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}$, GND
I_{OZB}	Maximum TRI-STATE Output Leakage @ B_n		5.5 5.5	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	$V_I = V_{IL}$, V_{IH}, $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum I_{CC}/Input	All Inputs	5.5	5.5	1.0	1.35	1.5	mA	$V_I = V_{CC} - 2.1V$
		B_n	5.5	3.6		0.35	0.5	mA	$V_I = V_{CCB} - 0.6V$
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		5.5	Open		8	80	μA	$A_n = V_{CCA}$ or GND B_n = Open, $\overline{OE} = V_{CCA}$ T/$\overline{R} = V_{CCA}$, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		5.5 5.5	3.6 5.5		8 8	80 80	μA	$A_n = V_{CCA}$ or GND $B_n = V_{CCB}$ or GND $\overline{OE}$ = GND, T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current		5.5 5.5	3.6 5.5		5 8	50 80	μA	$A_n = V_{CCA}$ or GND $B_n = V_{CCB}$ or GND $\overline{OE}$ = GND, T/$\overline{R} = V_{CCA}$
V_{OLPA}	Quiet Output Maximum Dynamic V_{OL}		5.0 5.0	3.3 5.0		1.5 1.5		V	(Notes 1 and 2)
V_{OLPB}			5.0 5.0	3.3 5.0		0.8 1.5		V	(Notes 1 and 2)
V_{OLVA}	Quiet Output Minimum Dynamic V_{OL}		5.0 5.0	3.3 5.0		−1.2 −1.2		V	(Notes 1 and 2)
V_{OLVB}			5.0 5.0	3.3 5.0		−0.8 −1.2		V	(Notes 1 and 2)
V_{IHDA}	Minimum High Level Dynamic Input Voltage		5.0 5.0	3.3 5.0		2.0 2.0		V	(Notes 1 and 3)
V_{IHDB}			5.0 5.0	3.3 5.0		2.0 3.5		V	(Notes 1 and 3)
V_{ILDA}	Maximum Low Level Dynamic Input Voltage		5.0 5.0	3.3 5.0		0.8 0.8		V	(Notes 1 and 3)
V_{ILDB}			5.0 5.0	3.3 5.0		0.8 1.5		V	(Notes 1 and 3)

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	74LVXC4245 $C_L = 50$ pF $V_{CCA} = 4.5V$ to $5.5V$ $V_{CCB} = 4.5V$ to $5.5V$					74LVXC4245 $C_L = 50$ pF $V_{CCA} = 4.5V$ to $5.5V$ $V_{CCB} = 2.7V$ to $3.6V$					Units
		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	4.9 4.0	6.5 5.5	1.0 1.0	7.0 6.0	1.0 1.0	5.5 5.0	7.5 7.0	1.0 1.0	8.0 7.5	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	4.7 3.9	6.5 5.0	1.0 1.0	7.0 5.5	1.0 1.0	5.6 4.3	7.5 6.0	1.0 1.0	8.0 6.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	5.6 5.7	7.5 7.5	1.0 1.0	8.0 8.0	1.0 1.0	6.7 6.9	9.0 9.5	1.0 1.0	10.0 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	7.4 6.1	9.0 7.5	1.0 1.0	10.0 8.5	1.0 1.0	8.0 6.3	10.0 8.0	1.0 1.0	11.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.8 3.8	7.0 5.5	1.0 1.0	7.5 6.0	1.0 1.0	6.0 4.2	9.0 6.5	1.0 1.0	9.5 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	3.4 2.9	5.5 4.5	1.0 1.0	6.0 5.0	1.0 1.0	3.4 2.9	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 3) Data to Output		1.0	1.5		1.5		1.0	1.5		1.5	ns

Note 1: Typical values at $V_{CCA} = 5V$, $V_{CCB} = 5V$ @25°C.

Note 2: Typical values at $V_{CCA} = 5V$, $V_{CCB} = 3.3V$ @25°C.

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

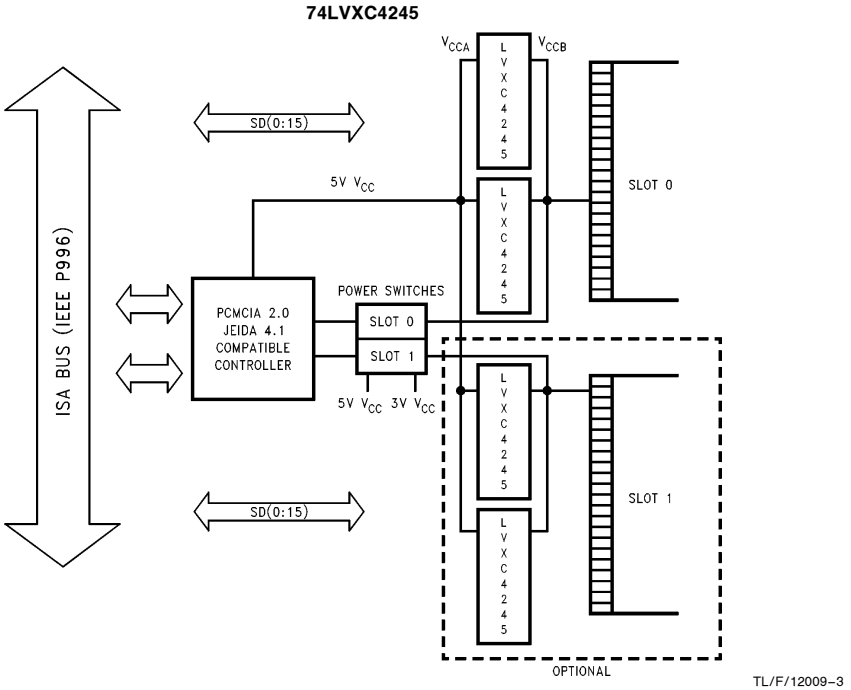
Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		10	pF	$V_{CCA} = 5V$, $V_{CCB} = 3.3V$
C_{PD}	Power Dissipation Capacitance	A → B	45	pF	$V_{CCA} = 5V$
		B → A	50	pF	$V_{CCB} = 3.3V$

Note: C_{PD} is measured at 10 MHz.

Configurable I/O Application for PCMCIA Cards

Block Diagram

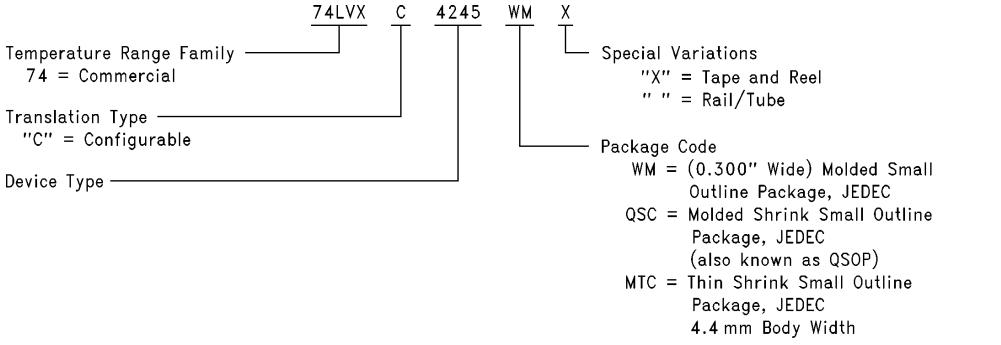


The LVXC4245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC4245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC4245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC4245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC4245 must always be tied to a 5V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the block diagram above, the LVXC4245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

74LVXC4245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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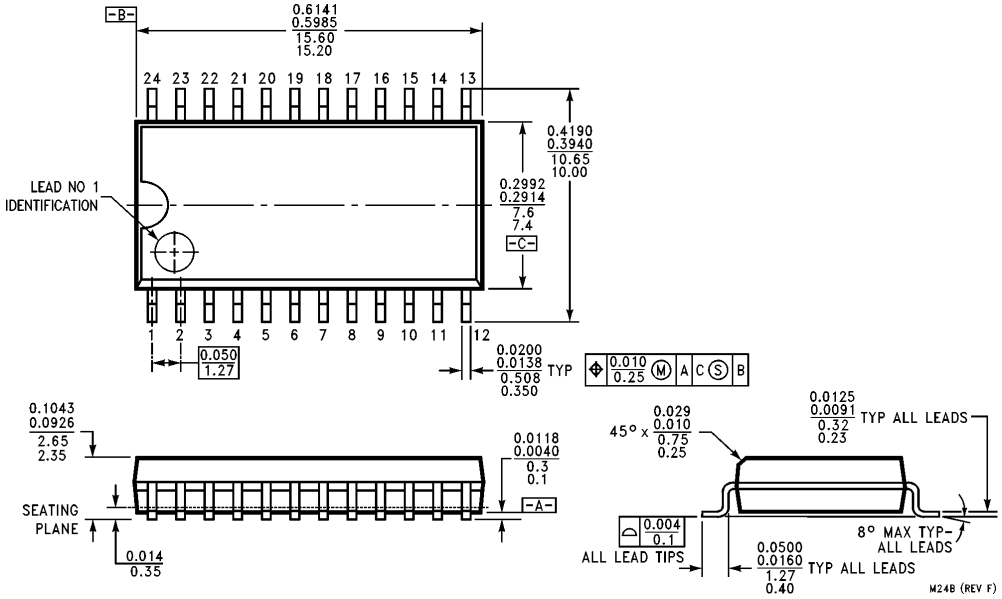
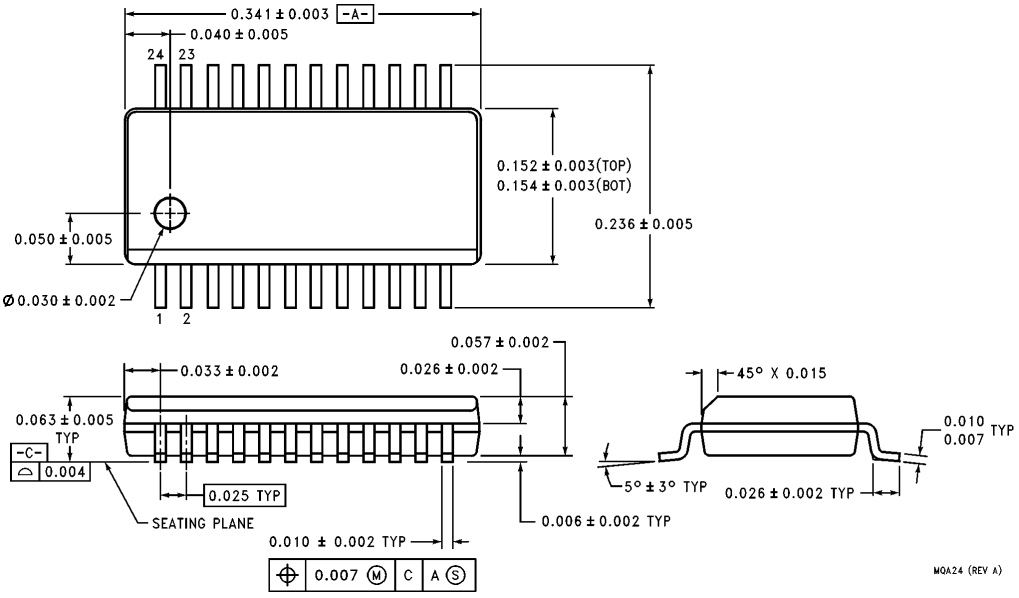
Physical Dimensions inches / millimeters



24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
Order Number 74LVXC4245WM or 74LVXC4245WMX
NS Package Number M24B

Physical Dimensions inches (Continued)



24-Lead (0.150″ Wide) Molded Shrink Small Outline Package, JEDEC
(also known as QSOP)
Order Number 74LVXC4245QSC or 74LVXC4245QSCX
NS Package Number MQA24

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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