National Semiconductor

October 1995

74LVX573
Low Voltage Octal Latch with TRI-STATE® Outputs

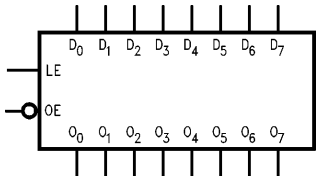
General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ, TSSOP and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Logic Symbols



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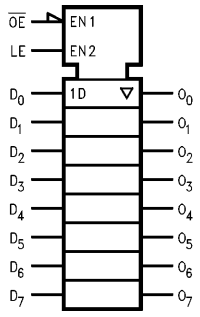
IEEE/IEC



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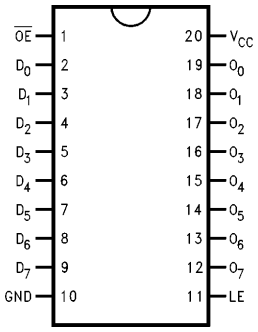
Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE 1	TSSOP
Order Number	74LVX573M 74LVX573MX	74LVX573SJ 74LVX573SJX	74LVX573MSCX	74LVX573MTC 74LVX573MTCX
See NS Package Number	M20B	M20D	MSC20	MTC20

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Functional Description

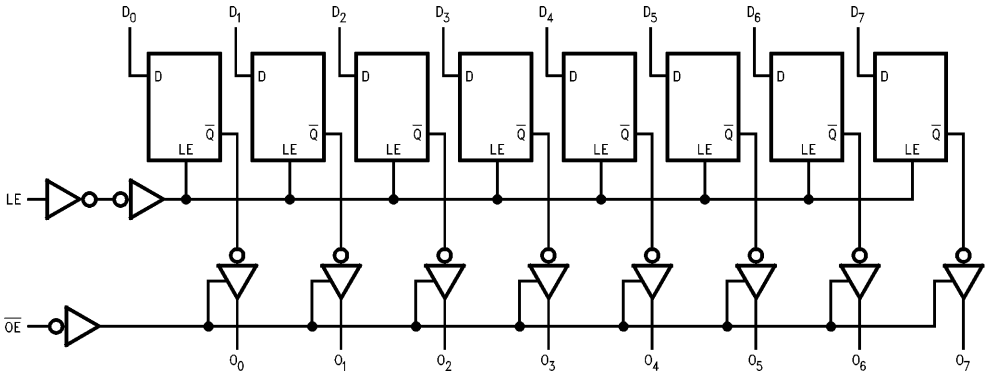
The LVX573 contains eight D-type latches with TRI-STATE® output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE® buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX573 T_A = +25°C			74LVX573 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX573 $T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX573 $T_A = +25°C$			74LVX573 $T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time D_n to O_n	2.7		7.6	14.5	1.0	17.5	ns	$C_L = 15$ pF
				10.1	18.0	1.0	21.0		$C_L = 50$ pF
		3.3 ±0.3		5.9	9.3	1.0	11.0		$C_L = 15$ pF
				8.4	12.8	1.0	14.5		$C_L = 50$ pF
t_{PLH} t_{PHL}	Propagation Delay Time LE to O_n	2.7		8.2	15.6	1.0	18.5	ns	$C_L = 15$ pF
				10.7	19.1	1.0	22.0		$C_L = 50$ pF
		3.3 ±0.3		6.4	10.1	1.0	12.0		$C_L = 15$ pF
				8.9	13.6	1.0	15.5		$C_L = 50$ pF
t_{PZL} t_{PZH}	TRI-STATE® Output Enable Time	2.7		7.8	15.0	1.0	18.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
				10.3	18.5	1.0	22.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		6.1	9.7	1.0	12.0		$C_L = 15$ pF, $R_L = 1$ kΩ
				8.6	13.2	1.0	15.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ} t_{PHZ}	TRI-STATE® Output Disable Time	2.7		12.1	19.1	1.0	22.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		10.1	13.6	1.0	15.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_W	LE Pulse Width	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
t_S	Setup Time D_n to LE	2.7	5.0			5.0		ns	
		3.3 ±0.3	3.5			3.5			
t_H	Hold Time D_n to LE	2.7	1.5			1.5		ns	
		3.3 ±0.3	1.5			1.5			
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	$C_L = 50$ pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

Capacitance

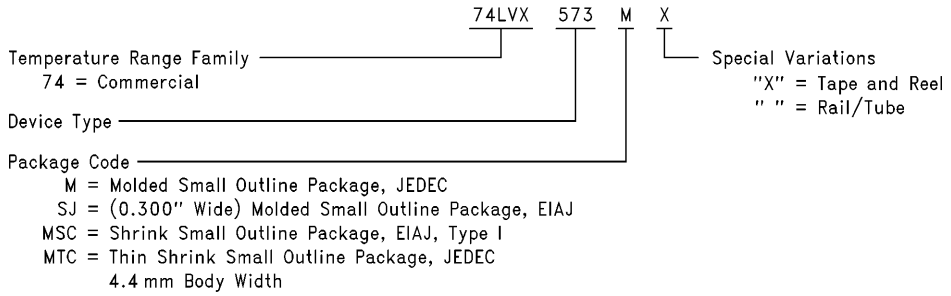
Symbol	Parameter	74LVX573			74LVX573		Units
		$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		27				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$

74LVX573 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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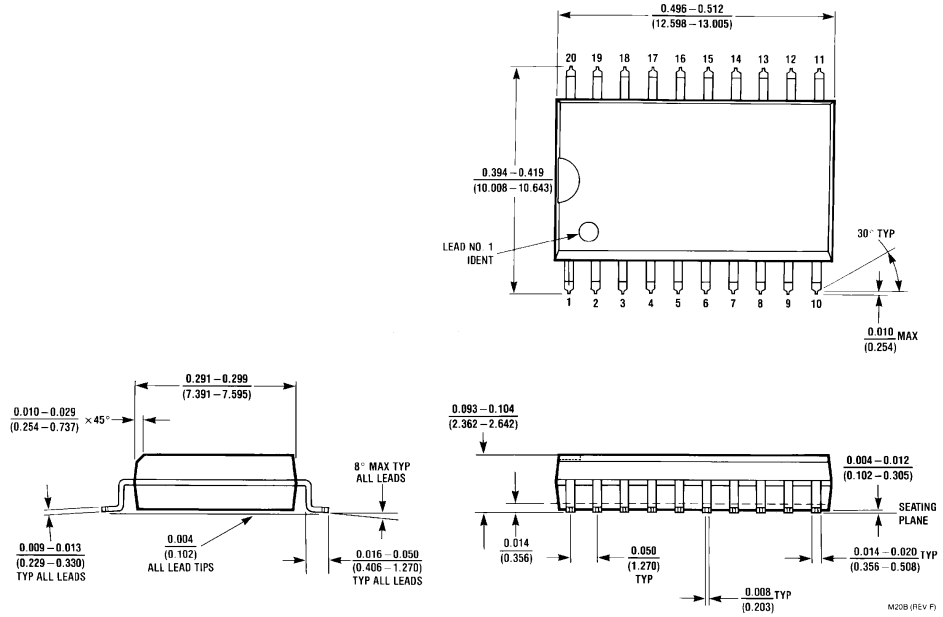
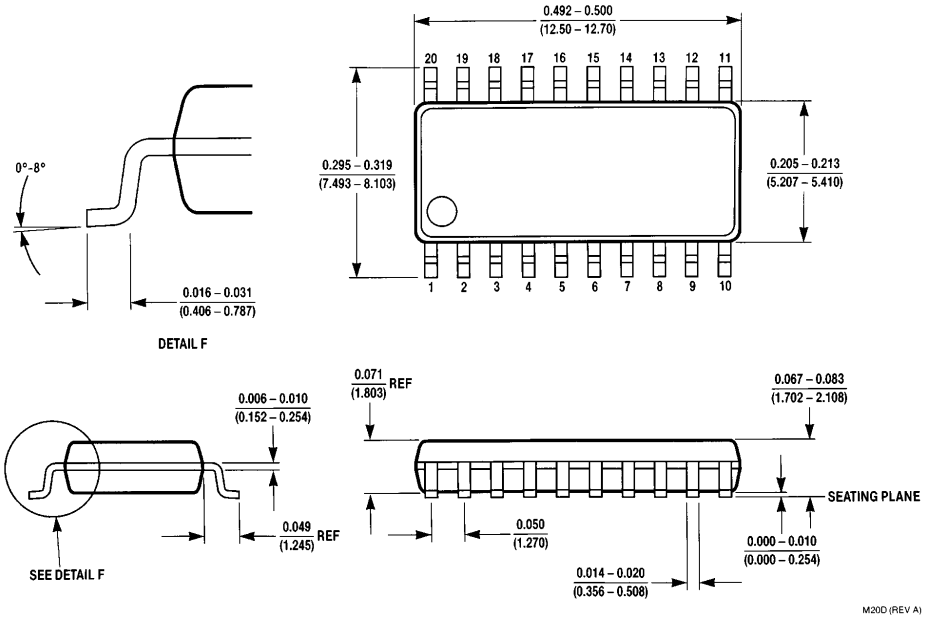
Physical Dimensions inches (millimeters)

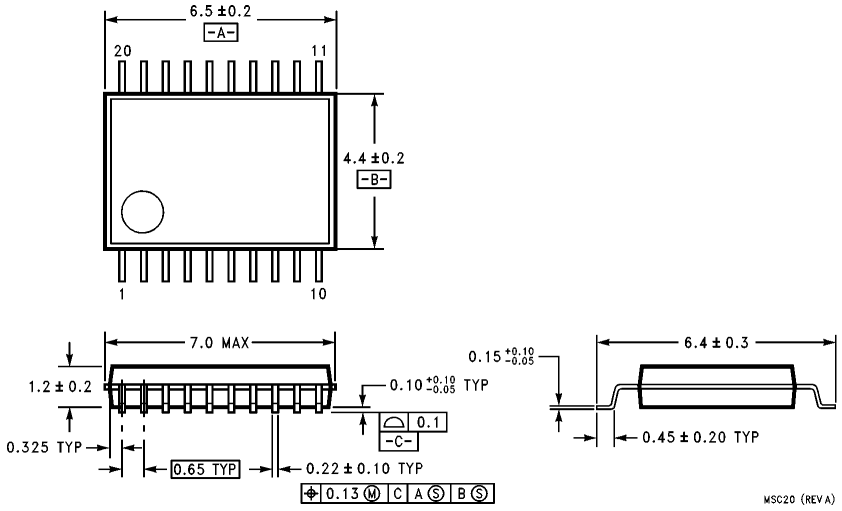


20-Lead Small Outline Integrated Circuit (M)
Order Number 74LVX573M or 74LVX573MX
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



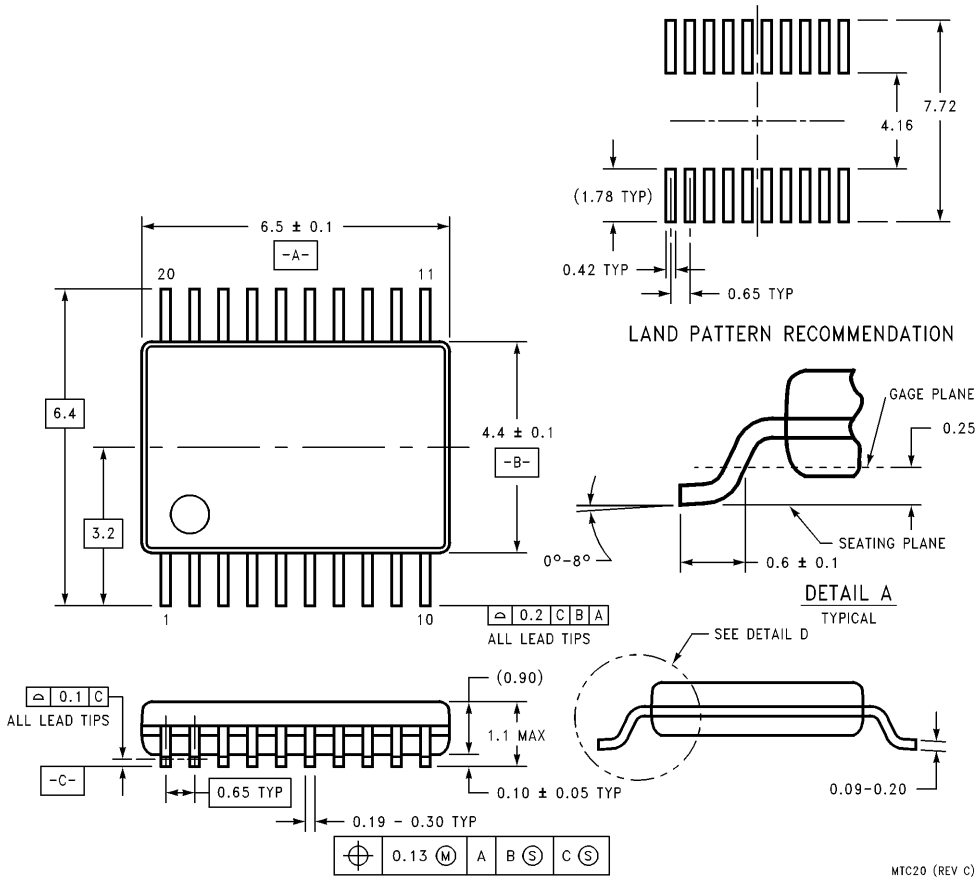
20-Lead Small Outline Package EIAJ SOIC (SJ)
Order Number 74LVX573SJ or 74LVX573SJX
NS Package Number M20D



All dimensions in millimeters

20-Lead Plastic EIAJ SSOP Type I (MSC)
Order Number 74LVX573MSCX
NS Package Number MSC20

Physical Dimensions inches (millimeters) (Continued)



20-Lead Thin Shrink Small Outline Package, JEDEC
Order Number 74LVX573MTC or 74LVX573MTCX
NS Package Number MTC20

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