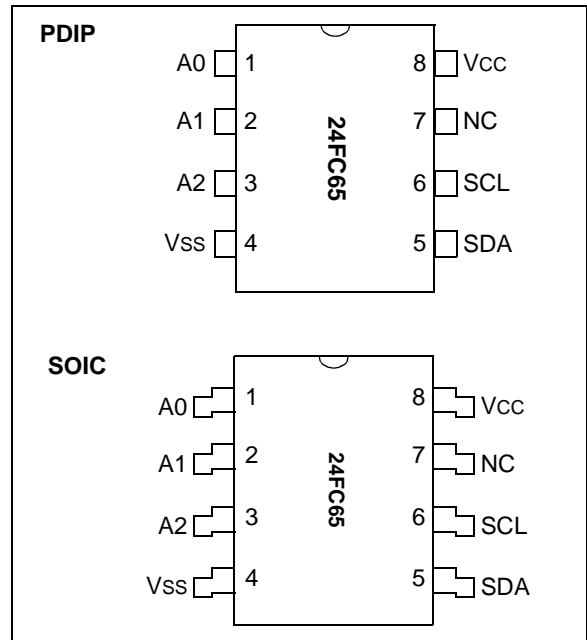# 24FC65

64K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM

FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- 1 MHz SE2.bus two wire protocol
- Up to eight devices may be connected to the same bus for up to 512K bits total memory
- Programmable block security options
- Programmable endurance options
- Schmitt trigger inputs for noise suppression
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles guaranteed for a 4K block
  - 1,000,000 E/W cycles guaranteed for a 60K block
- Variable page size up to 64 bytes
- 8 byte x 8 line input cache (64 bytes) for fast write loads
- <3 ms typical write cycle time, byte or page
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C):   0°C to +70°C
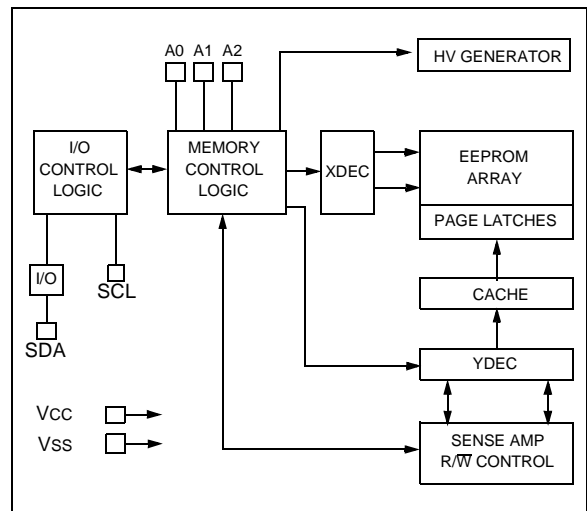 - Industrial (I):   -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 24FC65 is a "smart" 8K 8x 8 Serial Electrically Erasable PROM (EEPROM) with a high-speed 1MHz SE2.bus whose protocol is functionally equivalent to the industry-standard I²C bus. This device has been developed for advanced applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24FC65 offers a relocatable 4K-bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 ERASE/WRITE (E/W) cycles guaranteed. The 24FC65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional

PACKAGE TYPES

PDIP

A0	1	8	Vcc
A1	2	7	NC
A2	3	6	SCL
Vss	4	5	SDA

SOIC

A0	1	8	Vcc
A1	2	7	NC
A2	3	6	SCL
Vss	4	5	SDA

BLOCK DIAGRAM

address lines allow the connection of up to eight 24FC65's on the same bus for up to 512K bits contiguous EEPROM memory. The 24FC65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

24FC65

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc...7.0V
All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V
Storage temperature ....-65°C to +150°C
Ambient temp. with power applied ....-65°C to +125°C
Soldering temperature of leads (10 seconds) ....+300°C
ESD protection on all pins ....≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
					V_{CC} = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
A0, A1, A2, SCL and SDA pins: High level input voltage Low level input voltage Hysteresis of SCL and SDA Low level output voltage of SDA	V_{IH} V_{IL} V_{HYS} V_{OL}	0.7 V_{CC} — 0.05 V_{CC} —	— 0.3 V_{CC} — 0.40	V V V V	 (Note) I_{OL} = 3.0 mA
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = 0.1V to V_{CC}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = 0.1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{INT}	—	10	pF	V_{CC} = 5.0V (Note) Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} Write I_{CC} Read	— —	3 150	mA µA	V_{CC} = 5.5V, SCL = 1 MHz V_{CC} = 5.5V, SCL = 1 MHz
Standby current	I_{CCS}	—	5	µA	V_{CC} = 5.5V, SCL = SDA =V_{CC} A0, A1, A2 = V_{SS}

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP
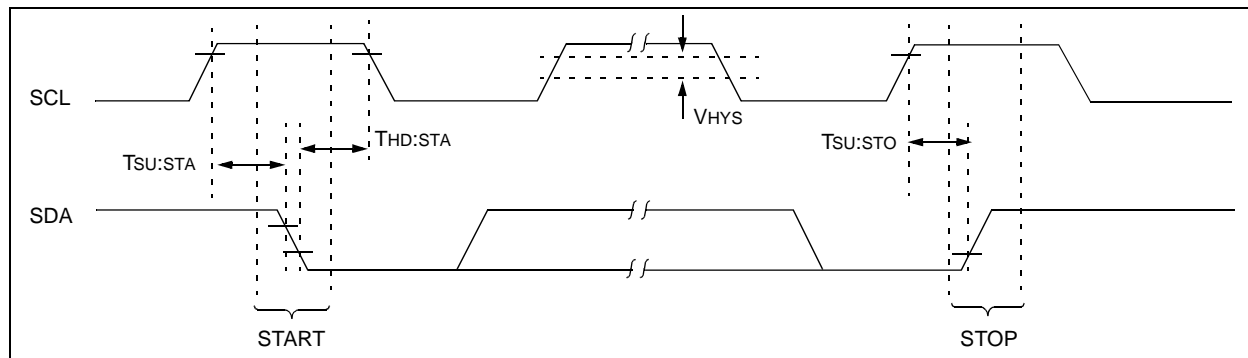
TABLE 1-3:   AC CHARACTERISTICS

Parameter	Symbol	1 MHz Bus		Units	Remarks
		Min	Max		
Clock frequency	F_{CLK}	0	1000	kHz	
Clock high time	T_{HIGH}	500	—	ns	
Clock low time	T_{LOW}	500	—	ns	
SDA and SCL rise time	T_R	—	300	ns	(Note 1)
SDA and SCL fall time	T_F	—	100	ns	(Note 1)
START hold time	$T_{HD:STA}$	250	—	ns	After this period the first clock pulse is generated
START setup time	$T_{SU:STA}$	250	—	ns	Only relevant for repeated START
Data input hold time	$T_{HD:DAT}$	0	—	ns	
Data input setup time	$T_{SU:DAT}$	100	—	ns	
STOP setup time	$T_{SU:STO}$	250	—	ns	
Output valid from clock	T_{AA}	—	350	ns	(Note 2)
Bus free time	T_{BUF}	500	—	ns	Time the bus must be free before a new transmission can start
Write cycle time	T_{WR}	—	5	ms/page	(Note 3)
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100 percent tested.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 100 ns) of the falling edge of SCL to avoid unintended generation of START or STOPs.

3: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2:   BUS TIMING DATA
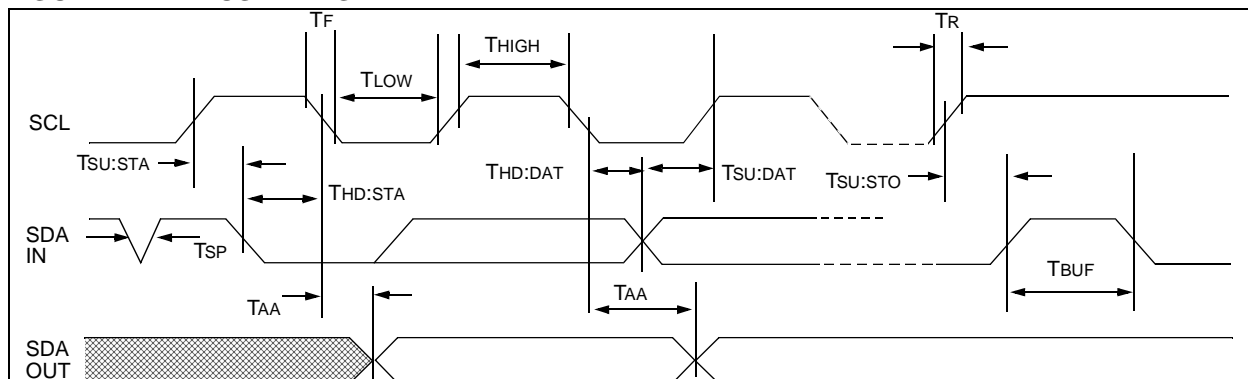
24FC65

2.0   FUNCTIONAL DESCRIPTION

The 24FC65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOPs, while the 24FC65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0   BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1   Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2   Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START. All commands must be preceded by a START.

3.3   Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP. All operations must be ended with a STOP.

3.4   Data Valid (D)

The state of the data line represents valid data when, after a START, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START and terminated with a STOP. The number of the data bytes transferred between the START and STOPs is determined by the master device.

3.5   Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

> **Note:**   The 24FC65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24FC65) must leave the data line HIGH to enable the master to generate the STOP.

**FIGURE 3-1:   DATA TRANSFER SEQUENCE ON THE SERIAL BUS**
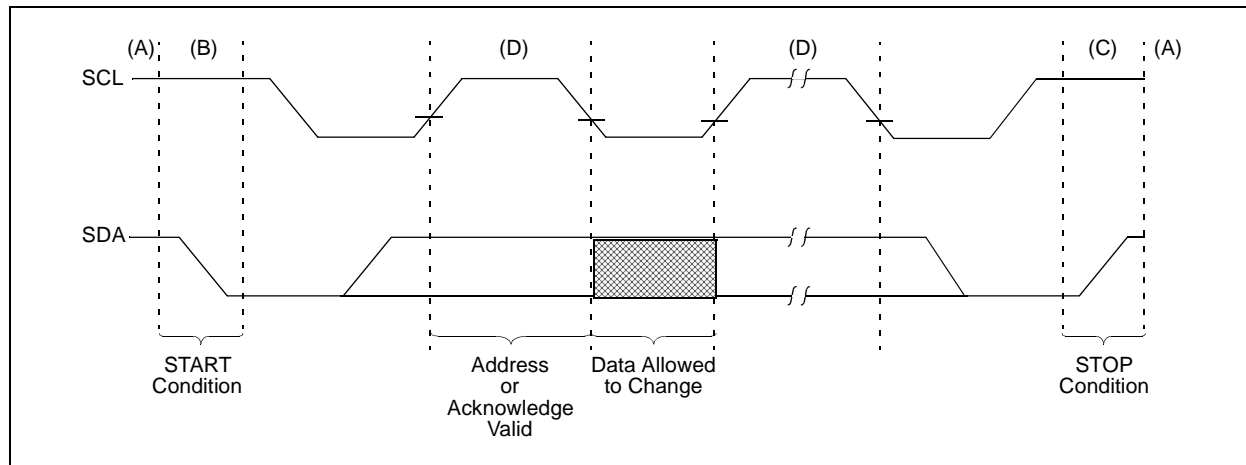
3.6   Device Addressing

A control byte is the first byte received following the START from the master device. The control byte consists of a four bit control code, for the 24FC65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transfered first.   Following the START, the 24FC65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24FC65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24FC65 will select a read or write operation.

| Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2:   CONTROL BYTE ALLOCATION

X = Don't care
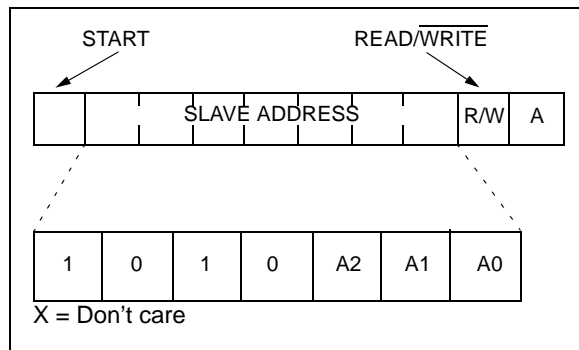
4.0   WRITE OPERATION

4.1   Byte Write

Following the START from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24FC65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24FC65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24FC65 the master device will transmit the data word to be written into the addressed memory location. The 24FC65 acknowledges again and the master generates a STOP. This initiates the internal write cycle, and during this time the 24FC65 will not generate acknowledge signals (Figure 4-1).

4.2   Page Write

The write control byte, word address and the first data byte are transmitted to the 24FC65 in the same way as in a byte write. But instead of generating a STOP the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24FC65. They will be written from the cache into the EEPROM array after the master has transmitted a STOP. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the STOP (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a STOP should be generated by the master. If a STOP is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The STOP can be sent at any time during the transfer. As with the byte write operation, once the STOP is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a STOP occurs or the operation is aborted (Figure 4-2).
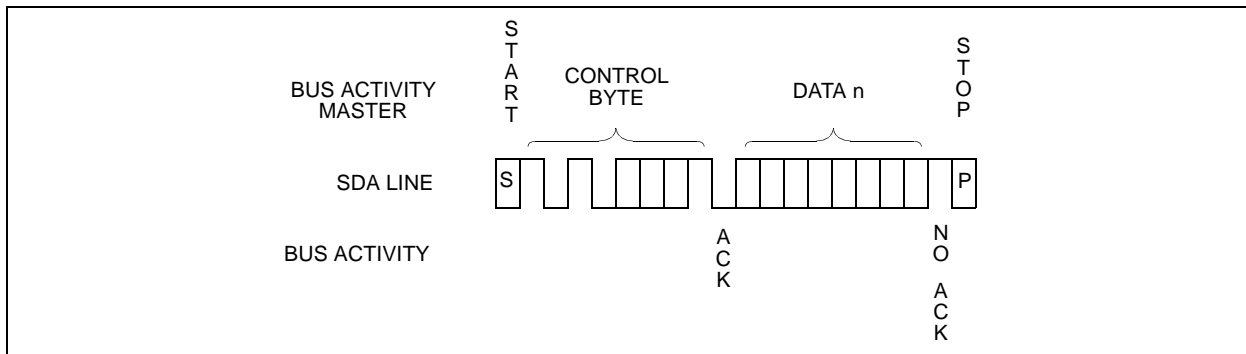
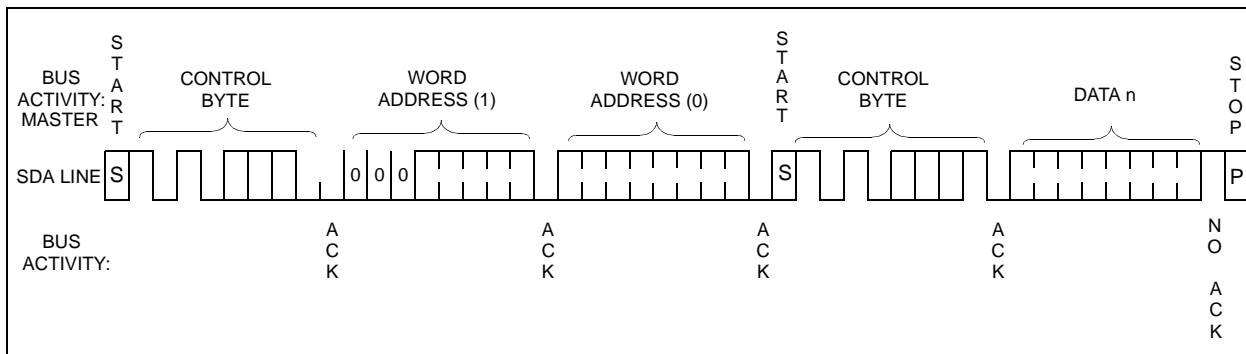**FIGURE 4-1:   BYTE WRITE**

24FC65
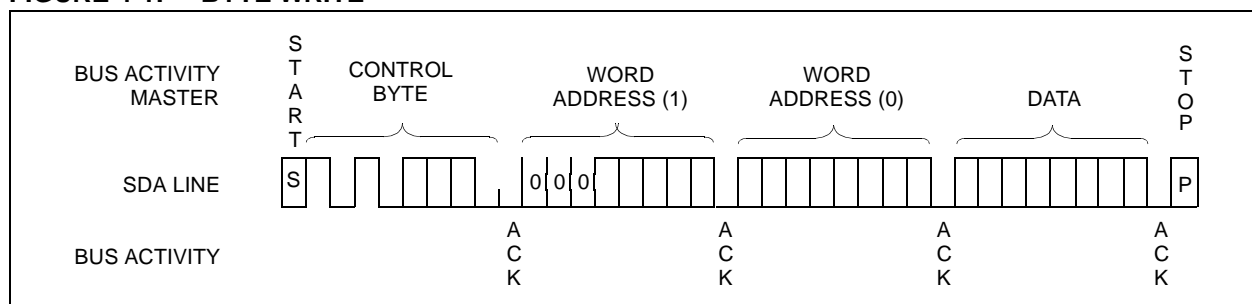
FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 7-1)
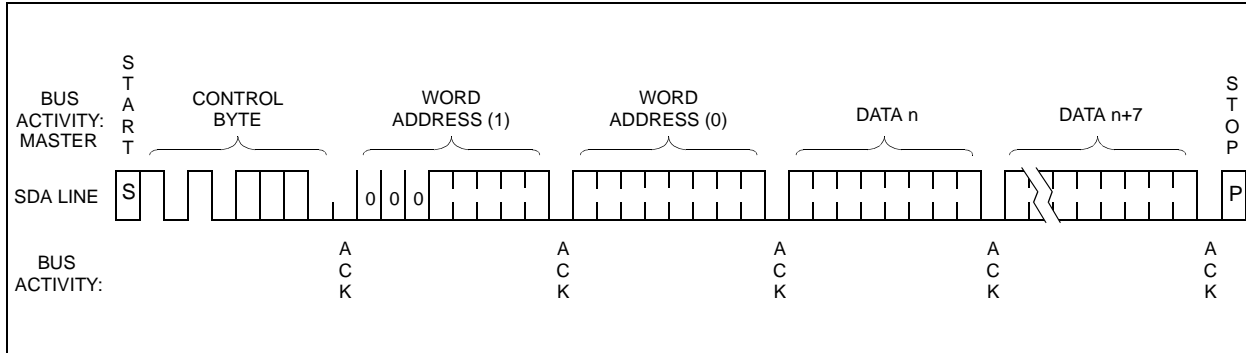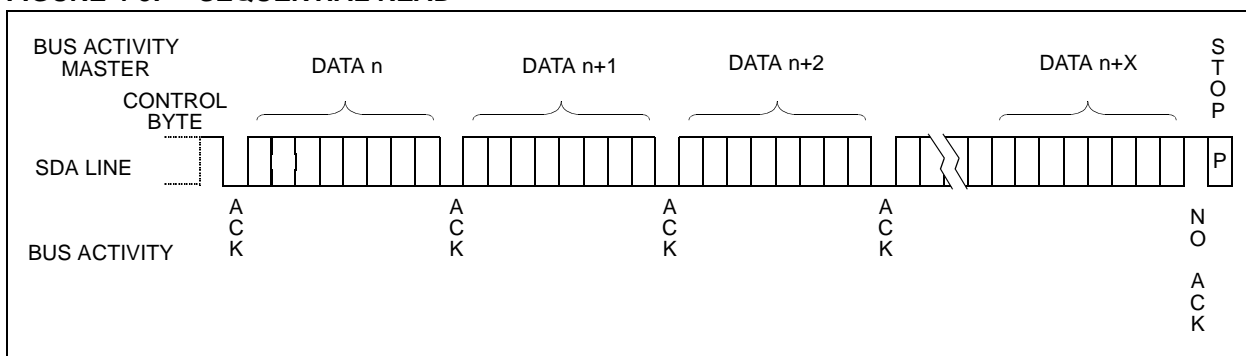
FIGURE 4-3: CURRENT ADDRESS READ

FIGURE 4-4: RANDOM READ

FIGURE 4-5: SEQUENTIAL READ

5.0   READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

5.1   Current Address Read

The 24FC65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24FC65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a STOP and the 24FC65 discontinues transmission (Figure 4-3).

5.2   Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24FC65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a START following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24FC65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a STOP which causes the 24FC65 to discontinue transmission (Figure 4-4).

5.3   Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24FC65 transmits the first data byte, the master issues an acknowledge as opposed to the STOP used in a random read. This acknowledge directs the 24FC65 to transmit the next sequentially addressed 8 bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a STOP.

To provide sequential reads the 24FC65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4   Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K-bits by adding up to eight 24FC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

5.5   Noise Protection

The SCL and SDA inputs incorporate Schmitt triggers which suppress noise spikes to assure proper device operation even on a noisy bus.

5.6   High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance (Figure 8-1). This block will be capable of 10,000,000 erase/write cycles guaranteed.

> **Note:** The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5.7   Security Options

The 24FC65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit7) of the first address byte set to a 1 (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit7 (S/$\overline{HE}$) set high and bit6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third

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byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

5.8   Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0   ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a START followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1:   ACKNOWLEDGE POLLING FLOW

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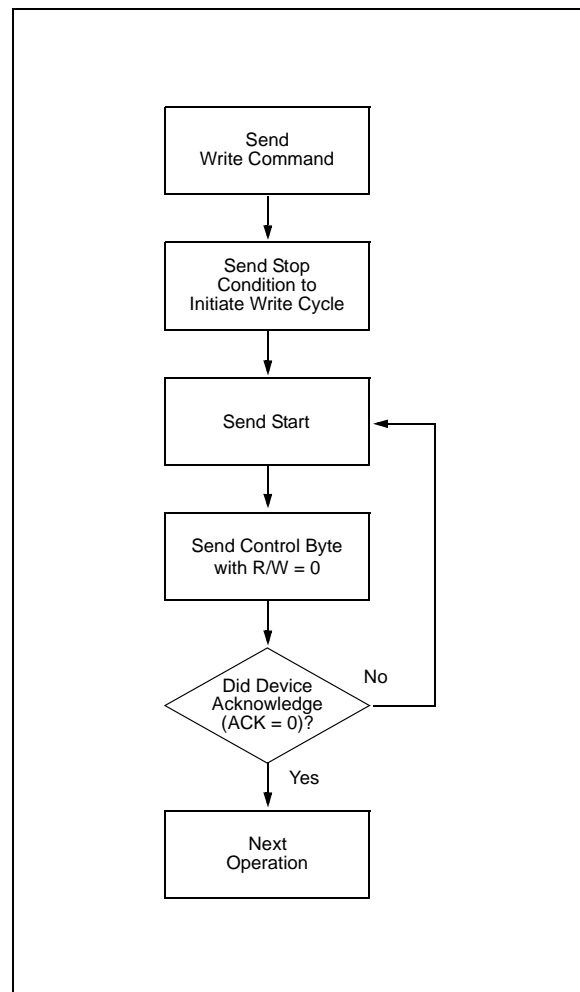
7.0   PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1   Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 7-1) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.
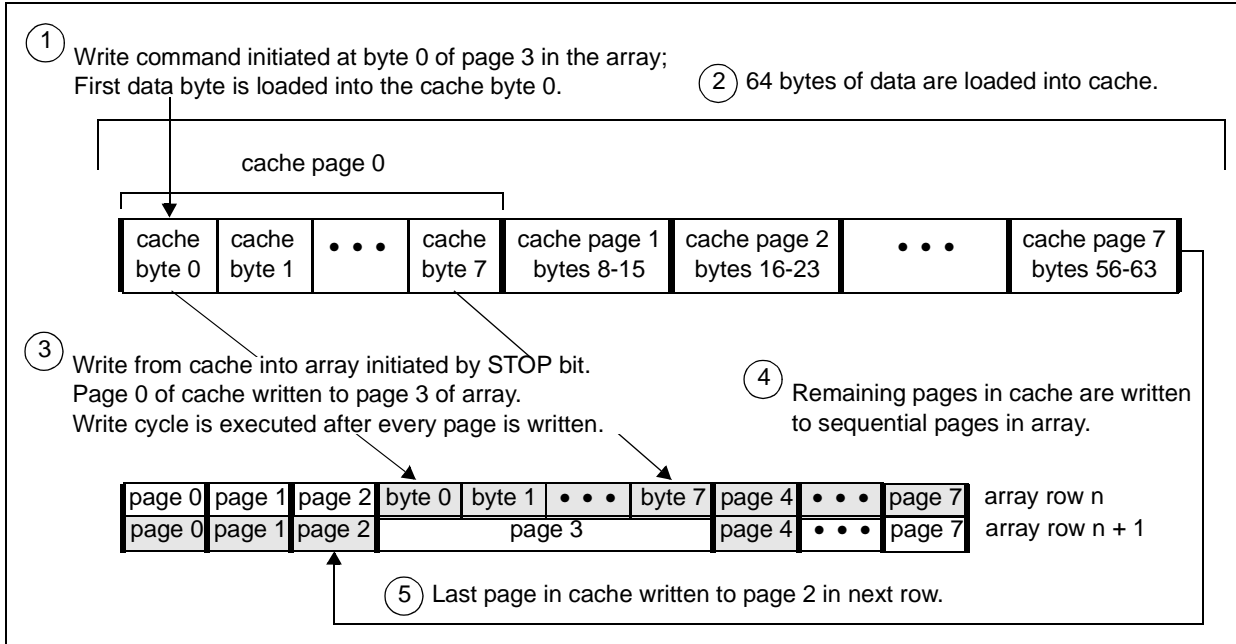
7.2   Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 7-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.
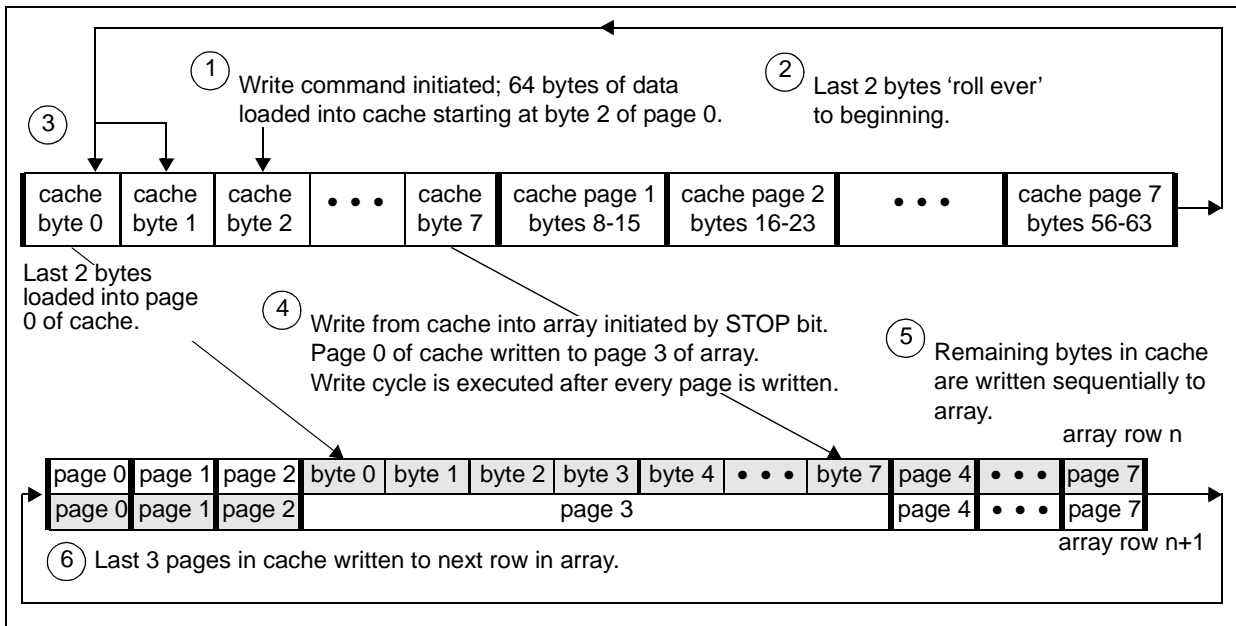
7.3   Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete.   This includes any error conditions, i.e. not receiving an acknowledge or STOP per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

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FIGURE 7-1:   CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

① Write command initiated at byte 0 of page 3 in the array;
First data byte is loaded into the cache byte 0.

② 64 bytes of data are loaded into cache.

cache page 0

| cache byte 0 | cache byte 1 | • • • | cache byte 7 | cache page 1 bytes 8-15 | cache page 2 bytes 16-23 | • • • | cache page 7 bytes 56-63 |

③ Write from cache into array initiated by STOP bit.
Page 0 of cache written to page 3 of array.
Write cycle is executed after every page is written.

④ Remaining pages in cache are written to sequential pages in array.

| page 0 | page 1 | page 2 | byte 0 | byte 1 | • • • | byte 7 | page 4 | • • • | page 7 | array row n |
| page 0 | page 1 | page 2 | page 3 | | | | page 4 | • • • | page 7 | array row n + 1 |

⑤ Last page in cache written to page 2 in next row.

FIGURE 7-2:   CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY

① Write command initiated; 64 bytes of data loaded into cache starting at byte 2 of page 0.

② Last 2 bytes 'roll ever' to beginning.

③

| cache byte 0 | cache byte 1 | cache byte 2 | • • • | cache byte 7 | cache page 1 bytes 8-15 | cache page 2 bytes 16-23 | • • • | cache page 7 bytes 56-63 |

Last 2 bytes loaded into page 0 of cache.

④ Write from cache into array initiated by STOP bit.
Page 0 of cache written to page 3 of array.
Write cycle is executed after every page is written.

⑤ Remaining bytes in cache are written sequentially to array.

array row n

| page 0 | page 1 | page 2 | byte 0 | byte 1 | byte 2 | byte 3 | byte 4 | • • • | byte 7 | page 4 | • • • | page 7 |
| page 0 | page 1 | page 2 | page 3 | | | | | | | page 4 | • • • | page 7 |

array row n+1

⑥ Last 3 pages in cache written to next row in array.

8.0   PIN DESCRIPTIONS

8.1   A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24FC65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2   SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 2 KΩ, must consider total bus capacitance and maximum rise/fall times).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOPs.

8.3   SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1:   CONTROL SEQUENCE BIT ASSIGNMENTS
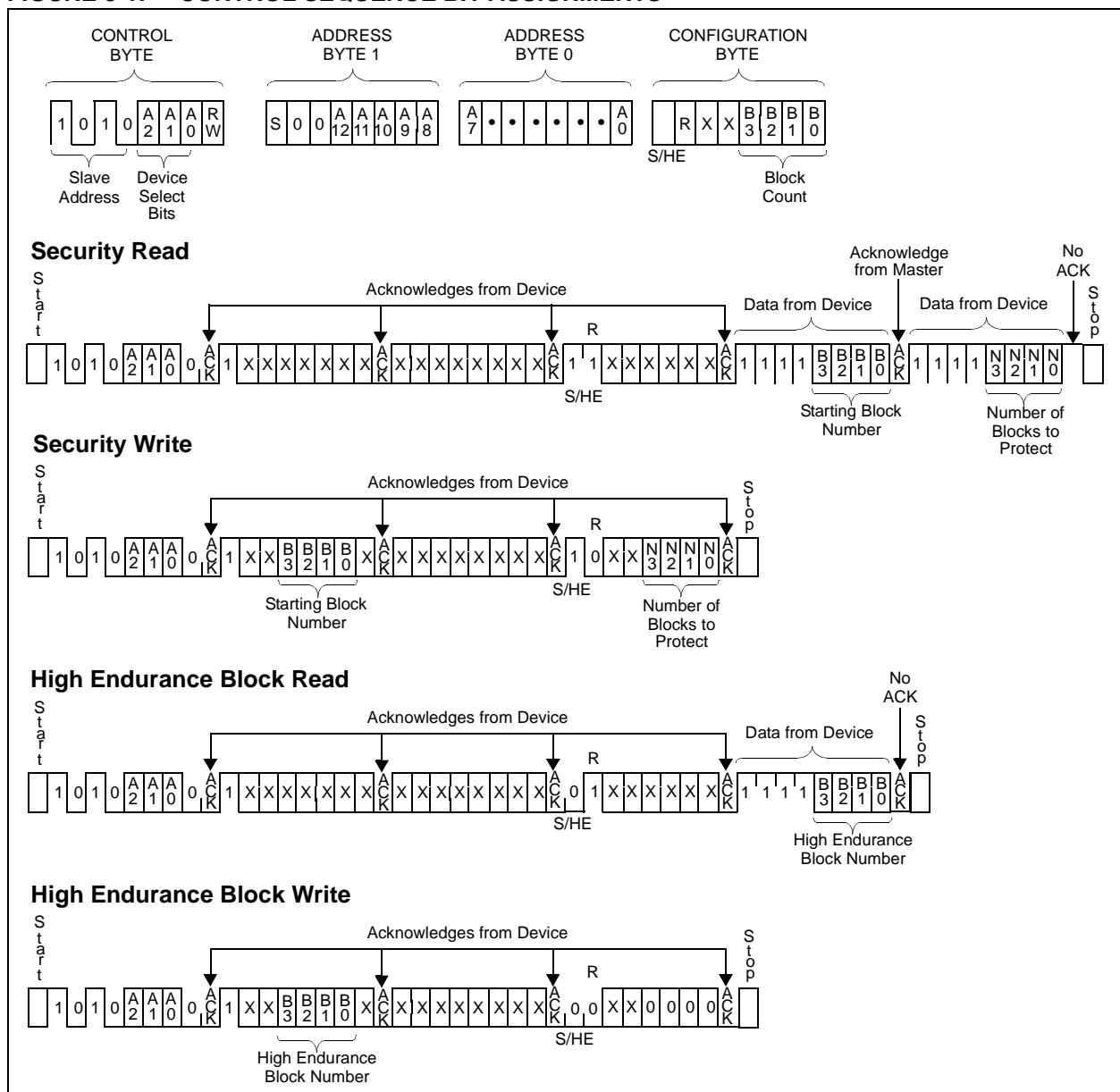
24FC65 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

24FC65 – **/P**

Package:
P = Plastic DIP (300 mil Body)
SM = Plastic SOIC (207 mil Body, EIAJ standard)

Temperature Range:
Blank = 0°C to +70°C
I = -40°C to +85°C

Device:
24FC65   64K, 1MHz I^{2}C Serial EEPROM
24FC65T   64K, 1MHz I^{2}C Serial EEPROM (Tape & Reel)
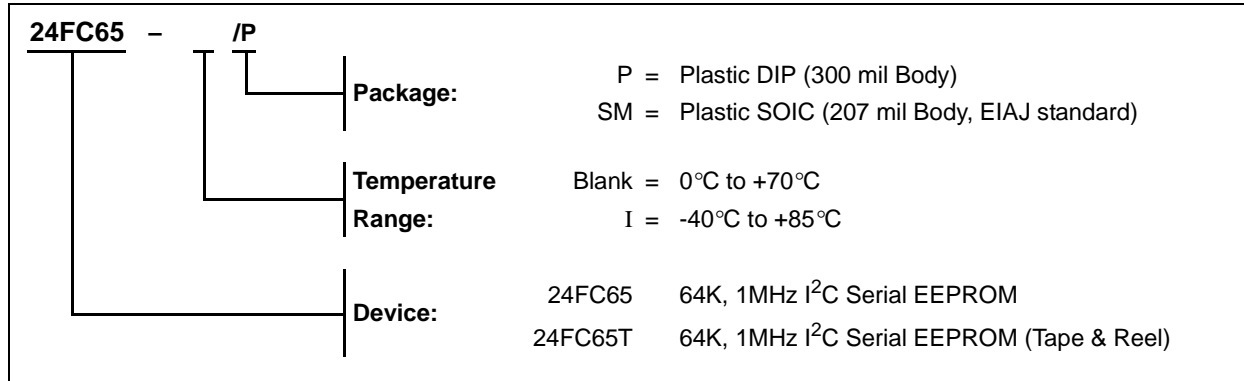
Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:
1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

• Microchip is willing to work with the customer who is concerned about the integrity of their code.

• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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