

## 64-Channel 8 MHz Serial-to-Parallel Converter with Push-Pull Outputs

### Features

- 5V CMOS Logic
- Up to 80V Output Voltage
- Low-power Level Shifting
- 8 MHz Data Rate
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR pin)
- Diode to  $V_{PP}$  allows Efficient Power Recovery
- Outputs may be Hot Switched

### Applications

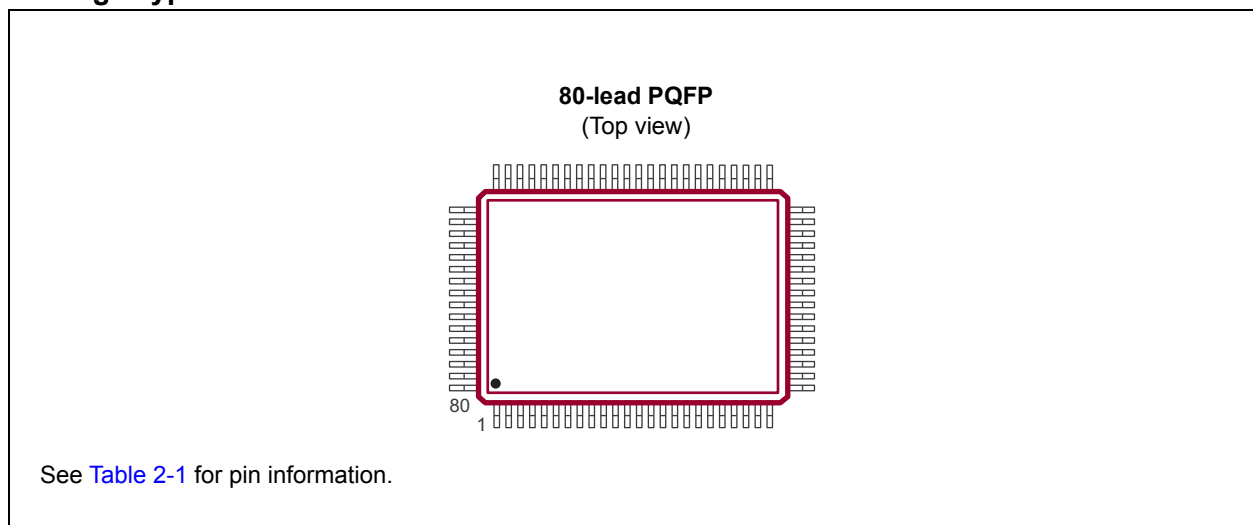
- Display Driver
- Vacuum Fluorescent Display Driver
- Inkjet Driver
- 3D Printer Driver
- Microelectromechanical Systems Applications

### General Description

The HV57908 is a low-voltage to high-voltage serial-to-parallel converter with 64 push-pull outputs. This device is designed as a driver for EL displays. It can also be used in any application requiring multiple-output high-voltage low-current sourcing-and-sinking capabilities, such as driving plasma panels, vacuum fluorescent displays and large matrix LCD displays.

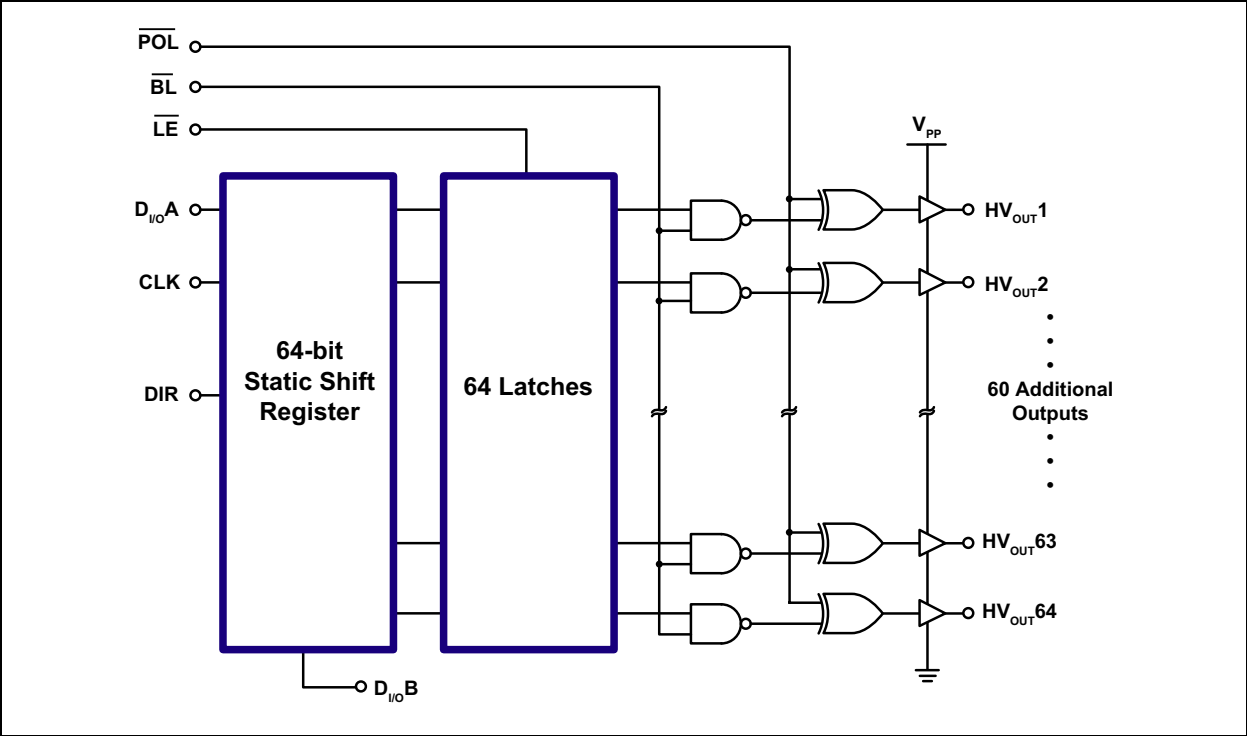
The device consists of a 64-bit Shift register, 64 latches and control logic to perform the polarity select and blanking of the outputs.  $HV_{OUT1}$  is connected to the first stage of the first Shift register through the polarity and blanking logic. Data is shifted through the Shift registers on the logic low-to-high transition of the clock. The DIR pin causes counter-clockwise shifting when connected to GND and clockwise shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register,  $HV_{OUT64}$ . The operation of the Shift register is not affected by the latch enable ( $\overline{LE}$ ), blanking ( $\overline{BL}$ ) and polarity ( $\overline{POL}$ ) inputs. Transfer of data from the Shift registers to the latches occurs when the  $\overline{LE}$  input is high. The data in the latches is stored when  $\overline{LE}$  is low.

### Package Type

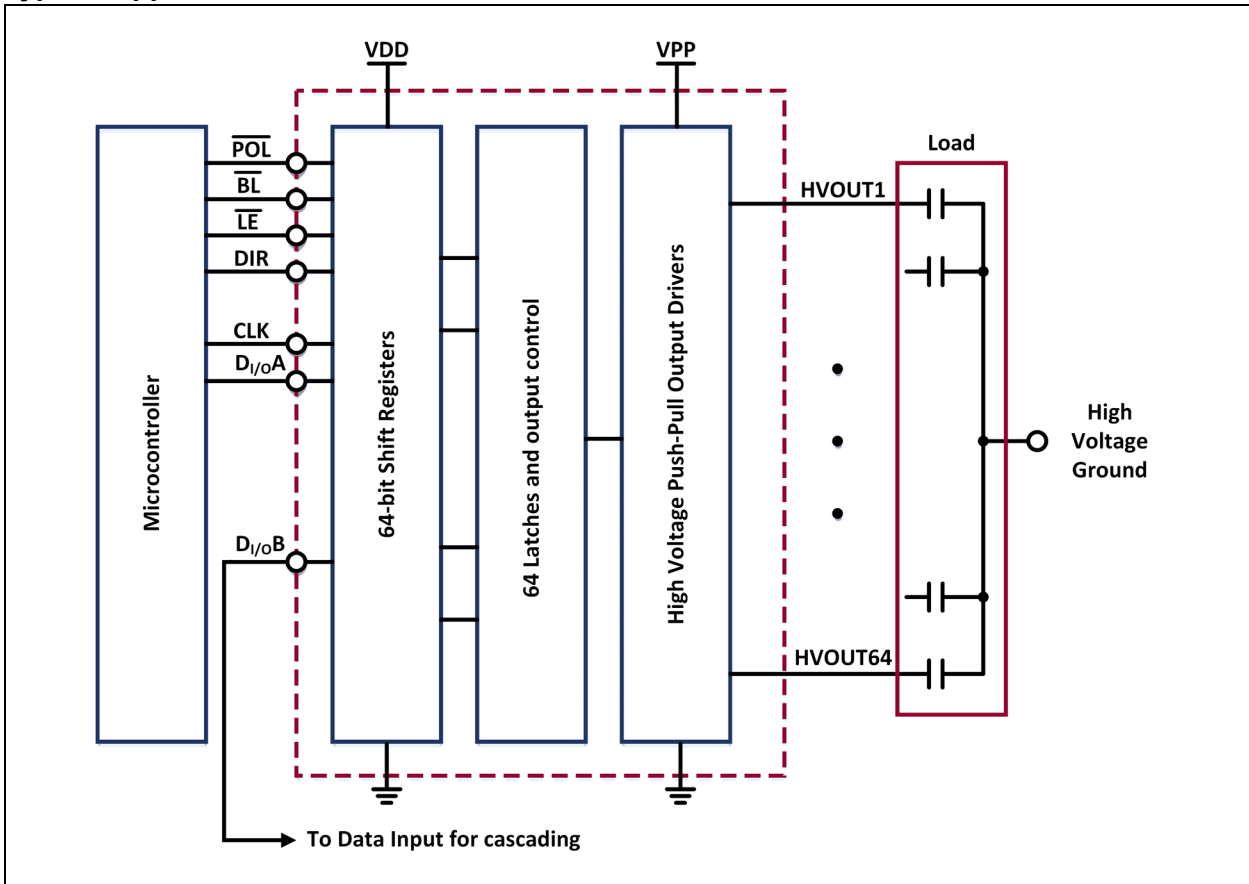


# HV57908

## Functional Block Diagram



## Typical Application Circuit



# HV57908

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage, $V_{DD}$ .....	-0.5V to +7.5V
Output Voltage, $V_{PP}$ .....	-0.5V to +90V
Logic Input Levels .....	-0.3V to $V_{DD}+0.3V$
Ground Current ( <b>Note 1</b> ) .....	1.5A
Maximum Junction Temperature, $T_{J(MAX)}$ .....	+125°C
Storage Temperature, $T_S$ .....	-65°C to +150°C
Continuous Total Power Dissipation:	
80-lead PQFP ( <b>Note 2</b> ) .....	1200 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Limited by the total power dissipated in the package

**Note 2:** For operations above 25°C ambient, derate linearly to the maximum operating temperature of 70°C at 20 mW/°C.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	$V_{DD}$	4.5	—	5.5	V	
Output Voltage	$V_{PP}$	8	—	80	V	
High-level Input Voltage	$V_{IH}$	$V_{DD}-0.5$	—	—	V	
Low-level Input Voltage	$V_{IL}$	0	—	0.5	V	
Clock Frequency per Register	$f_{CLK}$	—	—	8	MHz	
Operating Ambient Temperature	$T_A$	-40	—	+85	°C	

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Over recommended operating conditions unless otherwise noted,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
$V_{DD}$ Supply Current	$I_{DD}$	—	—	15	mA	$V_{DD} = V_{DD}$ maximum, $f_{CLK} = 8$ MHz	
Quiescent $V_{DD}$ Supply Current	$I_{DDQ}$	—	—	100	$\mu\text{A}$	All $V_{IN} = V_{DD}$	
High-voltage Supply Current	$I_{PP}$	—	—	100	$\mu\text{A}$	Outputs high	
		—	—	100	$\mu\text{A}$	Outputs low	
High-level Logic Input Current	$I_{IH}$	—	—	1	$\mu\text{A}$	$V_{IH} = V_{DD}$	
Low-level Logic Input Current	$I_{IL}$	—	—	-1	$\mu\text{A}$	$V_{IL} = 0\text{V}$	
High-level Output	HV <sub>OUT</sub>	$V_{OH}$	65	—	—	V	$V_{PP} = 80\text{V}$ , $I_O = -15$ mA
	Data Out		$V_{DD}-0.5$	—	—	V	$I_O = -100$ $\mu\text{A}$
Low-level Output	HV <sub>OUT</sub>	$V_{OL}$	—	—	7	V	$V_{PP} = 80\text{V}$ , $I_O = 12$ mA
	Data Out		—	—	0.5	V	$I_O = 100$ $\mu\text{A}$
High-voltage Clamp Diode Voltage	$V_{OC}$	—	—	1	V	$I_{OC} = 1$ mA	

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = +85^{\circ}\text{C}$  maximum. Logic signal inputs and data inputs have  $t_r, t_f \leq 5$  ns (10% and 90% points).

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	$f_{CLK}$	—	—	8	MHz	Per register
Clock Width High or Low	$t_{WL}, t_{WH}$	62	—	—	ns	
Data Set-up Time before Clock Rises	$t_{SU}$	10	—	—	ns	
Data Hold Time after Clock Rises	$t_H$	15	—	—	ns	
Time from Latch Enable to HV <sub>OUT</sub>	$t_{ON}, t_{OFF}$	—	—	500	ns	$C_L = 15$ pF
Latch Enable Pulse Width	$t_{WLE}$	25	—	—	ns	
Delay Time Clock to Latch Enable Low to High	$t_{DLE}$	25	—	—	ns	Note 1
Latch Enable Set-up Time before Clock Rises	$t_{SLE}$	0	—	—	ns	
Delay Time Clock to Data Low to High	$t_{DLH}$	—	—	70	ns	$C_L = 15$ pF
Delay Time Clock to Data High to Low	$t_{DHL}$	—	—	70	ns	$C_L = 15$ pF

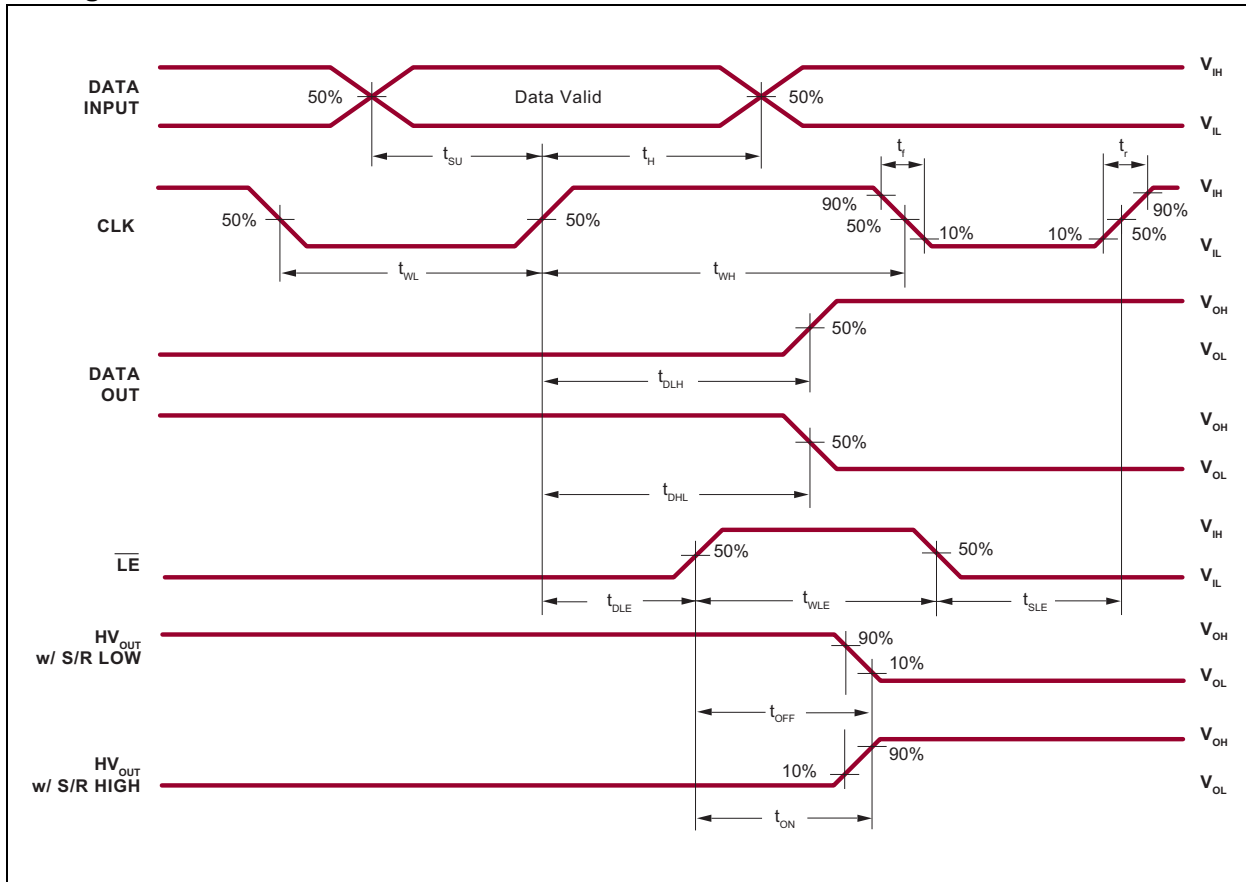
**Note 1:**  $t_{DLE}$  is not required but is recommended to produce stable high-voltage outputs and minimize power dissipation and current spikes.  $t_{DLE}$  allows the internal SR output to stabilize.

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-40	—	+85	$^{\circ}\text{C}$	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	$^{\circ}\text{C}$	
Storage Temperature	$T_S$	-65	—	+150	$^{\circ}\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
80-lead PQFP	$\theta_{JA}$	—	37	—	$^{\circ}\text{C/W}$	

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## Timing Waveforms



## 2.0 PIN DESCRIPTION

The details on the pins of HV57908 are listed on [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	HVOUT24/41	High-voltage output
2	HVOUT23/42	High-voltage output
3	HVOUT22/43	High-voltage output
4	HVOUT21/44	High-voltage output
5	HVOUT20/45	High-voltage output
6	HVOUT19/46	High-voltage output
7	HVOUT18/47	High-voltage output
8	HVOUT17/48	High-voltage output
9	HVOUT16/49	High-voltage output
10	HVOUT15/50	High-voltage output
11	HVOUT14/51	High-voltage output
12	HVOUT13/52	High-voltage output
13	HVOUT12/53	High-voltage output
14	HVOUT11/54	High-voltage output
15	HVOUT10/55	High-voltage output
16	HVOUT9/56	High-voltage output
17	HVOUT8/57	High-voltage output
18	HVOUT7/58	High-voltage output
19	HVOUT6/59	High-voltage output
20	HVOUT5/60	High-voltage output
21	HVOUT4/61	High-voltage output
22	HVOUT3/62	High-voltage output
23	HVOUT2/63	High-voltage output
24	HVOUT1/64	High-voltage output
25	DI/OA	Data Input/Output A pin
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	$\overline{LE}$	Latch enable pin
30	CLK	Clock pin
31	$\overline{BL}$	Blanking pin
32	VDD	Low-voltage supply voltage
33	DIR	Direction pin
34	GND	Ground

**Note:** Pin designation for DIR = H/L  
 Examples: For DIR = H, pin 41 is HVOUT64.  
 For DIR = L, pin 41 is HVOUT1.

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**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

Pin Number	Pin Name	Description
35	POL	Polarity pin
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	DI/OB	Data Input/Output B pin
40	VPP	High-voltage supply voltage
41	HVOUT64/1	High-voltage output
42	HVOUT63/2	High-voltage output
43	HVOUT62/3	High-voltage output
44	HVOUT61/4	High-voltage output
45	HVOUT60/5	High-voltage output
46	HVOUT59/6	High-voltage output
47	HVOUT58/7	High-voltage output
48	HVOUT57/8	High-voltage output
49	HVOUT56/9	High-voltage output
50	HVOUT55/10	High-voltage output
51	HVOUT54/11	High-voltage output
52	HVOUT53/12	High-voltage output
53	HVOUT52/13	High-voltage output
54	HVOUT51/14	High-voltage output
55	HVOUT50/15	High-voltage output
56	HVOUT49/16	High-voltage output
57	HVOUT48/17	High-voltage output
58	HVOUT47/18	High-voltage output
59	HVOUT46/19	High-voltage output
60	HVOUT45/20	High-voltage output
61	HVOUT44/21	High-voltage output
62	HVOUT43/22	High-voltage output
63	HVOUT42/23	High-voltage output
64	HVOUT41/24	High-voltage output
65	HVOUT40/25	High-voltage output
66	HVOUT39/26	High-voltage output
67	HVOUT38/27	High-voltage output
68	HVOUT37/28	High-voltage output
69	HVOUT36/29	High-voltage output
70	HVOUT35/30	High-voltage output
71	HVOUT34/31	High-voltage output
72	HVOUT33/32	High-voltage output
73	HVOUT32/33	High-voltage output

**Note:** Pin designation for DIR = H/L  
Examples: For DIR = H, pin 41 is HVOUT64.  
For DIR = L, pin 41 is HVOUT1.



**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

Pin Number	Pin Name	Description
74	HVOUT31/34	High-voltage output
75	HVOUT30/35	High-voltage output
76	HVOUT29/36	High-voltage output
77	HVOUT28/37	High-voltage output
78	HVOUT27/38	High-voltage output
79	HVOUT26/39	High-voltage output
80	HVOUT25/40	High-voltage output

**Note:** Pin designation for DIR = H/L  
Examples: For DIR = H, pin 41 is HVOUT64.  
For DIR = L, pin 41 is HVOUT1.

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## 3.0 FUNCTIONAL DESCRIPTION

Follow the steps in [Table 3-1](#) to power up and power down the HV57908.

**TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE**

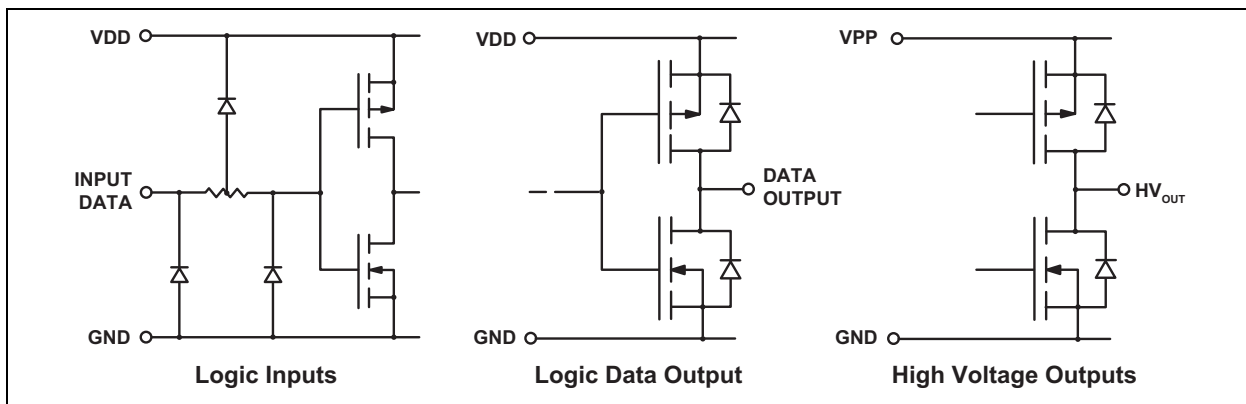
Power-up		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove $V_{PP}$ . ( <a href="#">Note 1</a> )
2	Apply $V_{DD}$ .	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove $V_{DD}$ .
4	Apply $V_{PP}$ . ( <a href="#">Note 1</a> )	4	Disconnect ground.

**Note 1:** The  $V_{PP}$  should not drop below  $V_{DD}$  or float during operation.

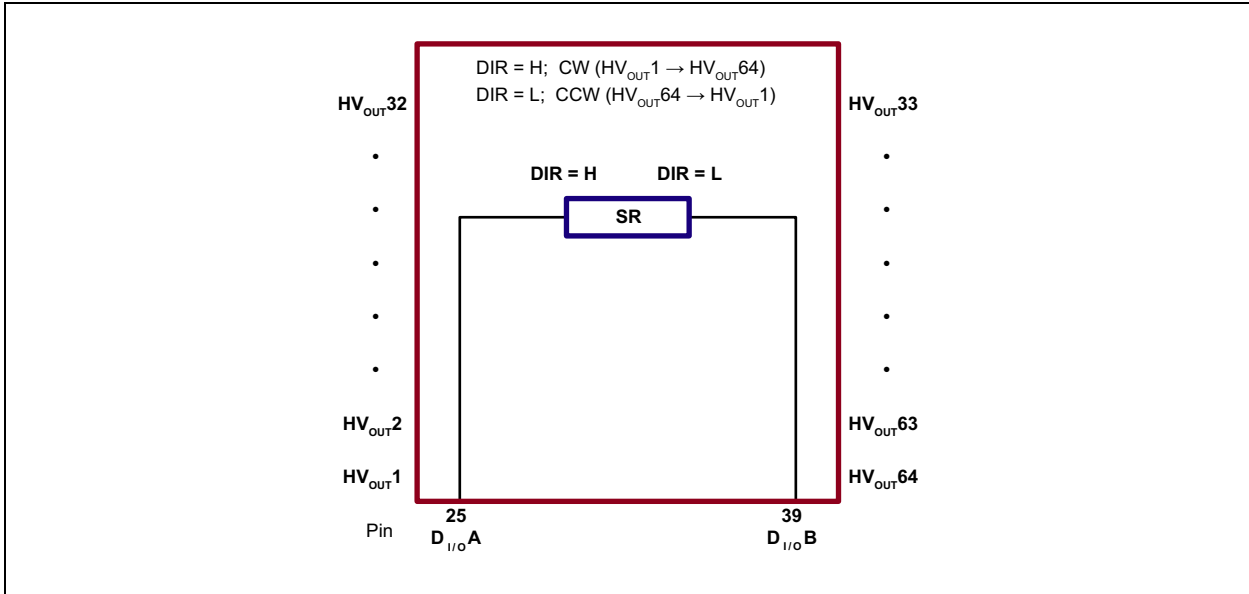
**TABLE 3-2: TRUTH FUNCTION TABLE**

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Register	High-voltage Output	Data Out
All O/P High	X	X	X	L	L	X	—	H	—
All O/P Low	X	X	X	L	H	X	—	L	—
O/P Normal	X	X	X	H	H	X	—	No inversion	—
O/P Inverted	X	X	X	H	L	X	—	Inversion	—
Data Falls through Latches (Latches Transparent)	L	↑	H	H	H	X	L	L	—
	H	↑	H	H	H	X	H	H	—
	L	↑	H	H	L	X	L	H	—
	H	↑	H	H	L	X	H	L	—
Data Stored/Latches Loaded	X	X	L	H	H	X	*	Stored data	—
	X	X	L	H	L	X	*	Inversion of stored data	—
I/O Relation	$D_{I/OA}$	↑	X	X	X	H	$Q_N \rightarrow Q_{N+1}$	—	$D_{I/OB}$
	$D_{I/OB}$	↑	X	X	X	L	$Q_N \rightarrow Q_{N-1}$	—	$D_{I/OA}$

**Note:**  
 H = High-logic level  
 L = Low-logic level  
 X = Irrelevant  
 ↑ = Low-to-high transition  
 \* = Dependent on the previous stage's state



**FIGURE 3-1:** Input and Output Equivalent Circuits.

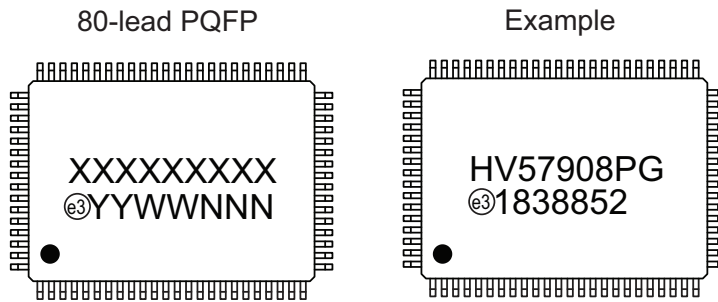


**FIGURE 3-2:** Shift Register Operation.

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## 4.0 PACKAGE MARKING INFORMATION

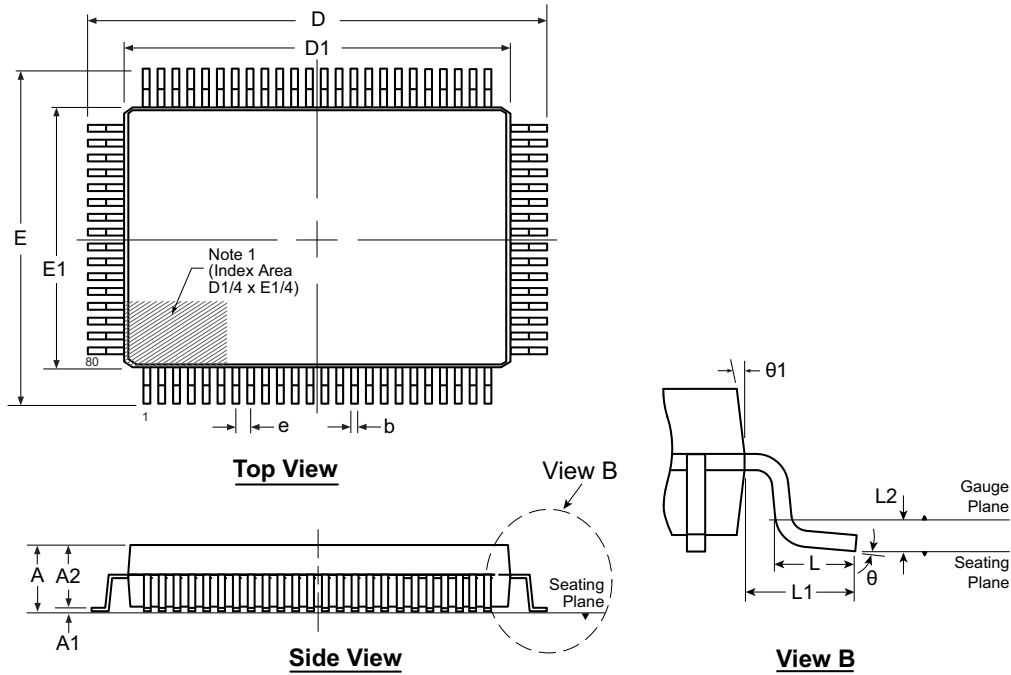
### 4.1 Packaging Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 80-Lead PQFP Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Note:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	$\theta$	$\theta_1$	
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88		3.5°	-	
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03		7°	16°	

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept. 1995.

\* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (January 2018)

- Converted Supertex Doc # DSFP-HV57908 to Microchip DS20005877A
- Removed “HVCMOS<sup>®</sup> Technology” from the Features section
- Changed the package marking format
- Made minor changes throughout the document

# HV57908

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV57908	=	64-Channel 8 MHz Serial-to-Parallel Converter with Push-Pull Outputs		
Package:	PG	=	80-lead PQFP		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	66/Tray for a PG Package		

**Example:**

a) HV57908PG-G: 64-Channel 8 MHz Serial-to-Parallel Converter with Push-Pull Outputs, 80-lead PQFP, 66/Tray



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