HV507

64-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs

Features

- Up to 300V Output Voltage
- Low-power Level Shifting from 5V to 300V
- Shift Register Speed:
  - 8 MHz at V_{DD} = 5V
- Latched Data Outputs
- Output Polarity and Blanking
- CMOS-compatible Inputs
- Forward and Reverse Shifting Options

Applications

- Display Driver
- Print Head Driver
- Microelectromechanical Systems Applications

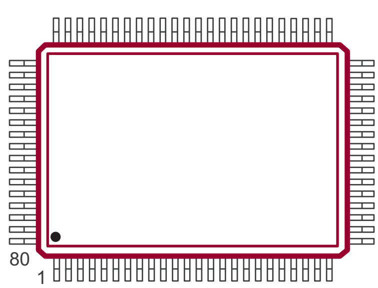
General Description

The HV507 is a low-voltage to high-voltage serial-to-parallel converter with 64 push-pull outputs. This device is designed as a printer driver for electrostatic applications. It can also be used in any application requiring multiple-output high-voltage low-current sourcing-and-sinking capabilities.

The device consists of a 64-bit Shift register, 64 latches and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With the DIR grounded, $D_{IO}A$ is data in and $D_{IO}B$ is data out. Data is shifted from $HV_{OUT}64$ to $HV_{OUT}1$. When DIR is at logic high, $D_{IO}B$ is data in and $D_{IO}A$ is data out. The data is then shifted from $HV_{OUT}1$ to $HV_{OUT}64$ through the Shift register on the low-to-high transition of the clock. Data output buffers are provided for cascading devices. The operation of the shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$) and polarity ($\overline{POL}$) inputs. Transfer of data from the Shift register to the latch occurs when the $\overline{LE}$ is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

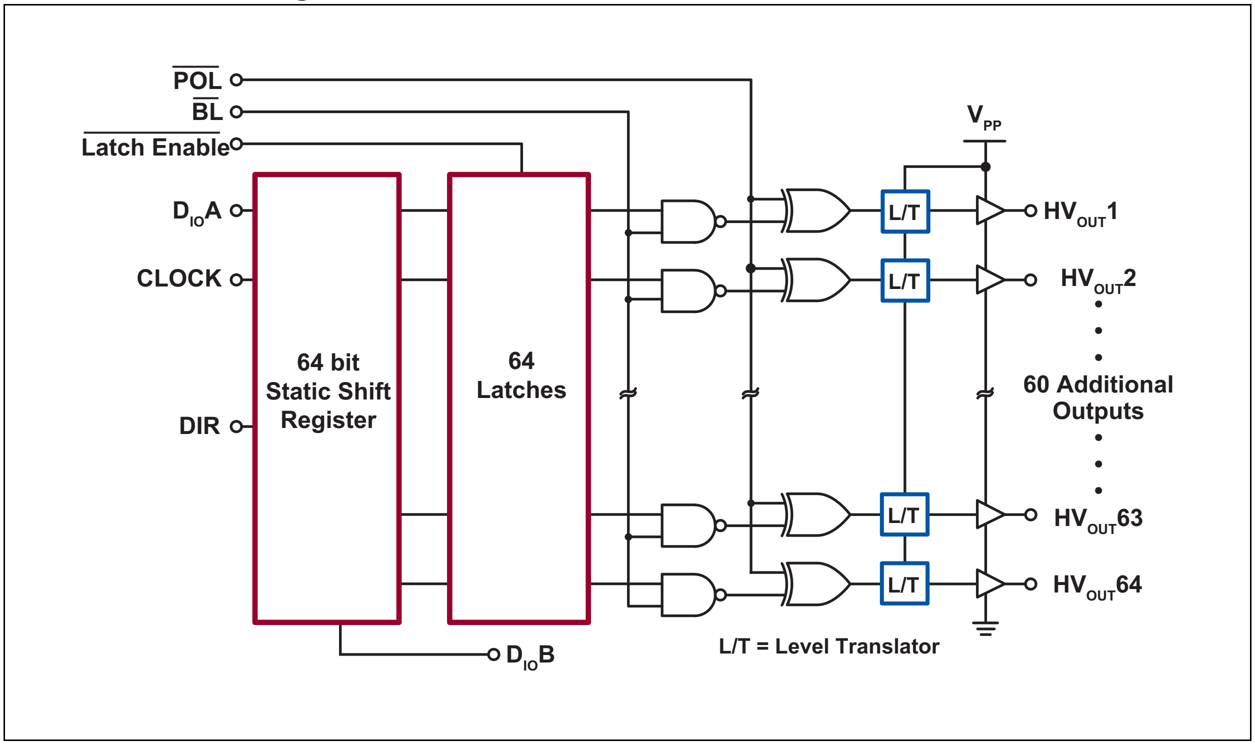
Package Type

80-lead PQFP
(Top view)

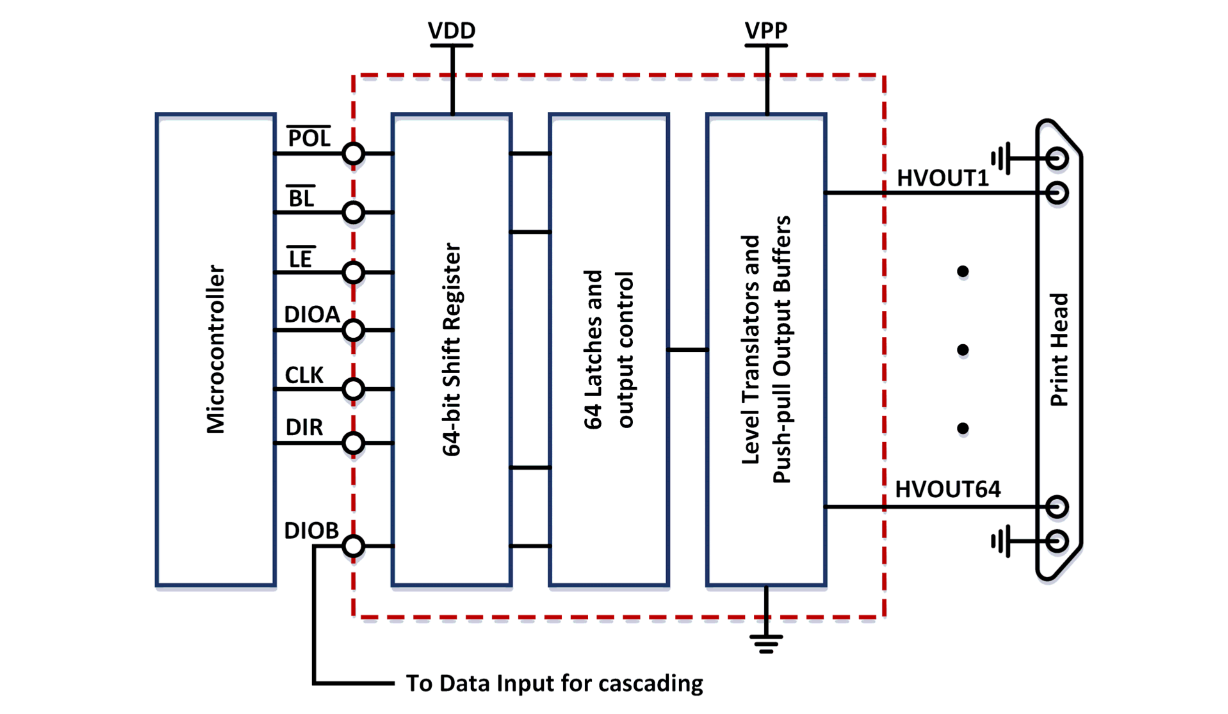


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Low-supply Voltage, V_{DD} .... –0.5V to +6V
High-supply Voltage, V_{PP} .... V_{DD} to +320V
Logic Input Levels .... –0.5V to V_{DD}+0.5V
Ground Current (**Note 2**) 0.5A
High-voltage Supply Current (**Note 1**) 0.5A
Operating Ambient Temperature, T_A .... 0°C to +70°C
Storage Temperature, T_S .... –65°C to +150°C
Continuous Total Power Dissipation:
80-lead PQFP (**Note 2**) .... 1200 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
2: For operations above 25°C ambient, derate linearly to 70°C at 26.7 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V	
High-voltage Supply Voltage	V_{PP}	60	—	300	V	
High-level Input Voltage	V_{IH}	V_{DD}–0.9V	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	0.9	V	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: For V_{DD} = 5V, V_{PP} = 300V and T_A = 25°C.							
Parameter		**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{DD} Supply Current		I_{DD}	—	—	15	mA	f_{CLK} = 8 MHz, f_{DATA} = 4 MHz, $\overline{LE}$ = low
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	200	µA	All V_{IN} = 0V or V_{DD}
High-voltage Supply Current		I_{PP}	—	—	0.5	mA	V_{PP} = 300V, all outputs high
			—	—	0.5	mA	V_{PP} = 300V, all outputs low
High-level Logic Input Current		I_{IH}	—	—	10	µA	V_{IN} = V_{DD}
Low-level Logic Input Current		I_{IL}	—	—	–10	µA	V_{IN} = 0V
High-level Output	HV_{OUT}	V_{OH}	265	—	—	V	V_{PP} = 300V, IHV_{OUT} = –1 mA, ID_{OUT} = –100 µA
	Data Out		V_{DD} –1	—	—	V	
Low-level Output	HV_{OUT}	V_{OL}	—	—	35	V	V_{DD} = 5V, IHV_{OUT} = 1 mA, ID_{OUT} = 100 µA
	Data Out		—	—	1	V	
HV_{OUT} Clamp Voltage		V_{OC}	—	—	V_{PP} + 1.5	V	I_{OL} = 1 mA
			—	—	–30	V	I_{OL} = –1 mA

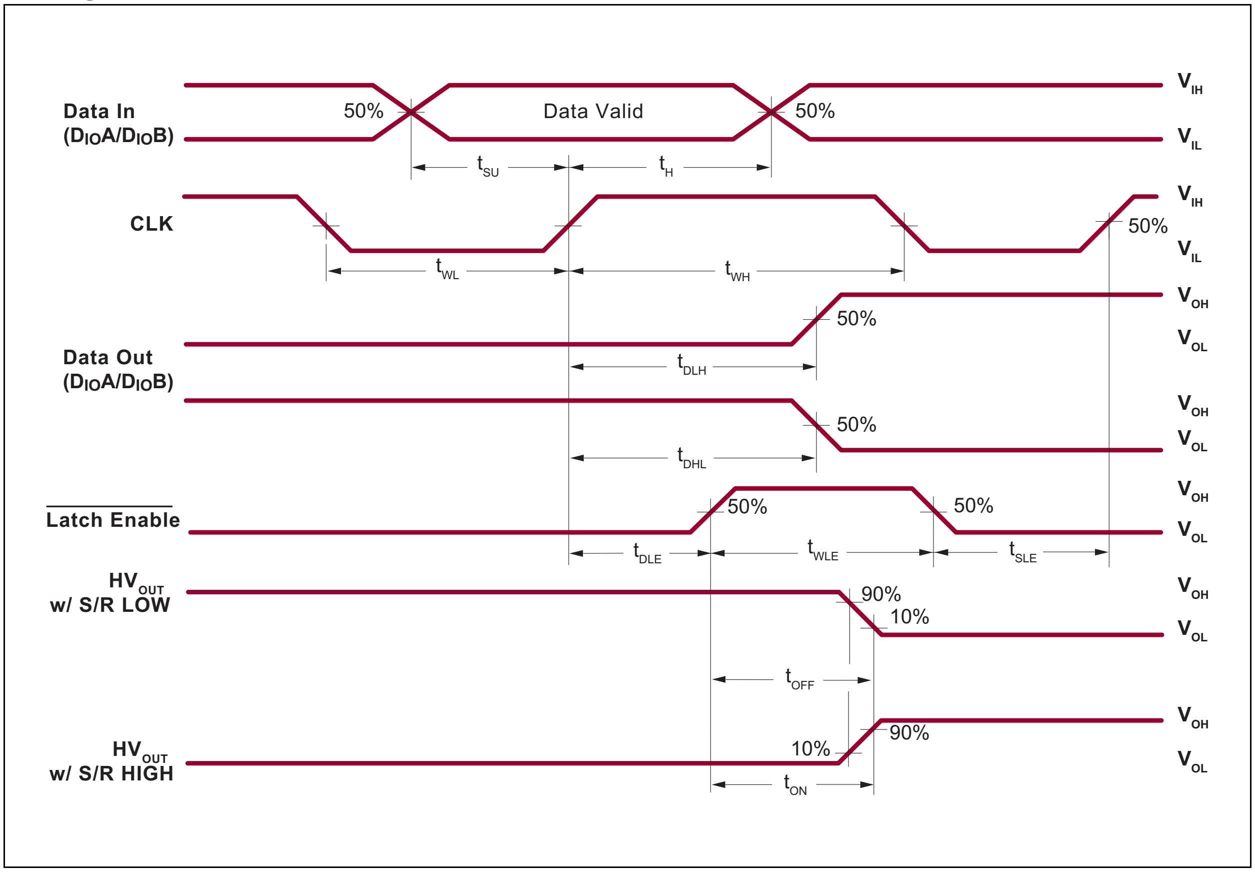
AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: For V_{DD} = 5V, V_{PP} = 300V and T_A = 25°C. Shift register speed can be as low as DC as long as data set-up and hold time meet the specifications.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Clock Frequency	f_{CLK}	—	—	8	MHz	
Clock Width High or Low	t_{WL}, t_{WH}	62	—	—	ns	
Data Set-up Time before Clock Rises	t_{SU}	35	—	—	ns	
Data Hold Time after Clock Rises	t_H	30	—	—	ns	
Time from Latch Enable to HV_{OUT}	t_{ON}, t_{OFF}	—	—	4	ns	C_L = 20 pF
Latch Enable Pulse Width	t_{WLE}	80	—	—	ns	
Delay Time Clock to Latch Enable Low to High	t_{DLE}	35	—	—	ns	
Latch Enable Set-up Time before Clock Rises	t_{SLE}	40	—	—	ns	
Delay Time Clock to Data Low to High	t_{DLH}	—	—	125	ns	C_L = 20 pF
Delay Time Clock to Data High to Low	t_{DHL}	—	—	125	ns	C_L = 20 pF
All Logic Inputs	t_r, t_f	—	—	5	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	+70	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
80-lead PQFP	θ_{JA}	—	37	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV507 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT41	High-voltage output
2	HVOUT42	High-voltage output
3	HVOUT43	High-voltage output
4	HVOUT44	High-voltage output
5	HVOUT45	High-voltage output
6	HVOUT46	High-voltage output
7	HVOUT47	High-voltage output
8	HVOUT48	High-voltage output
9	HVOUT49	High-voltage output
10	HVOUT50	High-voltage output
11	HVOUT51	High-voltage output
12	HVOUT52	High-voltage output
13	HVOUT53	High-voltage output
14	HVOUT54	High-voltage output
15	HVOUT55	High-voltage output
16	HVOUT56	High-voltage output
17	HVOUT57	High-voltage output
18	HVOUT58	High-voltage output
19	HVOUT59	High-voltage output
20	HVOUT60	High-voltage output
21	HVOUT61	High-voltage output
22	HVOUT62	High-voltage output
23	HVOUT63	High-voltage output
24	HVOUT64	High-voltage output
25	VPP	High-voltage power supply
26	DIOA	Serial Data Input/Output A
27	NC	No connection
28	NC	No connection
29	$\overline{BL}$	Blanking
30	$\overline{POL}$	Polarity
31	VDD	Low-voltage power supply
32	DIR	Direction
33	GND	Logic voltage ground
34	HVGND	High-voltage power supply
35	NC	No connection
36	NC	No connection

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	CLK	Data Shift Register Clock. Inputs are shifted into the Shift register on the positive edge of the clock.
38	$\overline{LE}$	Latch Enable
39	DIOB	Serial Data Input/Output B
40	VPP	High-voltage power supply
41	HVOUT1	High-voltage output
42	HVOUT2	High-voltage output
43	HVOUT3	High-voltage output
44	HVOUT4	High-voltage output
45	HVOUT5	High-voltage output
46	HVOUT6	High-voltage output
47	HVOUT7	High-voltage output
48	HVOUT8	High-voltage output
49	HVOUT9	High-voltage output
50	HVOUT10	High-voltage output
51	HVOUT11	High-voltage output
52	HVOUT12	High-voltage output
53	HVOUT13	High-voltage output
54	HVOUT14	High-voltage output
55	HVOUT15	High-voltage output
56	HVOUT16	High-voltage output
57	HVOUT17	High-voltage output
58	HVOUT18	High-voltage output
59	HVOUT19	High-voltage output
60	HVOUT20	High-voltage output
61	HVOUT21	High-voltage output
62	HVOUT22	High-voltage output
63	HVOUT23	High-voltage output
64	HVOUT24	High-voltage output
65	HVOUT25	High-voltage output
66	HVOUT26	High-voltage output
67	HVOUT27	High-voltage output
68	HVOUT28	High-voltage output
69	HVOUT29	High-voltage output
70	HVOUT30	High-voltage output
71	HVOUT31	High-voltage output
72	HVOUT32	High-voltage output
73	HVOUT33	High-voltage output
74	HVOUT34	High-voltage output
75	HVOUT35	High-voltage output
76	HVOUT36	High-voltage output

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
77	HVOUT37	High-voltage output
78	HVOUT38	High-voltage output
79	HVOUT39	High-voltage output
80	HVOUT40	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV507.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove V_{PP}. (**Note 1**)
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove V_{DD}.
4	Apply V_{PP}. (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} or float during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs				
	Data	**CLK**	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	**DIR**	**Shift Register 1**	**Shift Register 2...64**	**High-voltage Output 1**	**High-voltage Output 2...64**	**Data Out** *
All On	X	X	X	L	L	X	*	*...*	H	H...H	*
All Off	X	X	X	L	H	X	*	*...*	L	L...L	*
Invert Mode	X	X	L	H	L	X	*	*...*	$\overline{*}$	$\overline{*}...\overline{*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*...*	*	*...*	*
Store Data in Latches	X	X	↓	H	H	X	*	*...*	*	*...*	*
	X	X	↓	H	L	X	*	*...*	$\overline{*}$	$\overline{*}...\overline{*}$	*
Transparent Latch Mode	L	↑	H	H	H	X	L	*...*	L	*...*	*
	H	↑	H	H	H	X	H	*...*	H	*...*	*
I/O Relation	$D_{IO}A$	↑	X	X	X	L	Q_N→	Q_{N+1}	—		$D_{IO}B$
	$D_{IO}B$	↑	X	X	X	H	Q_N→	Q_{N+1}	—		$D_{IO}A$

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↑ = Low-to-high transition
↓ = High-to-low transition
* = Dependent on the previous stage's state before the last CLK or last $\overline{LE}$ high

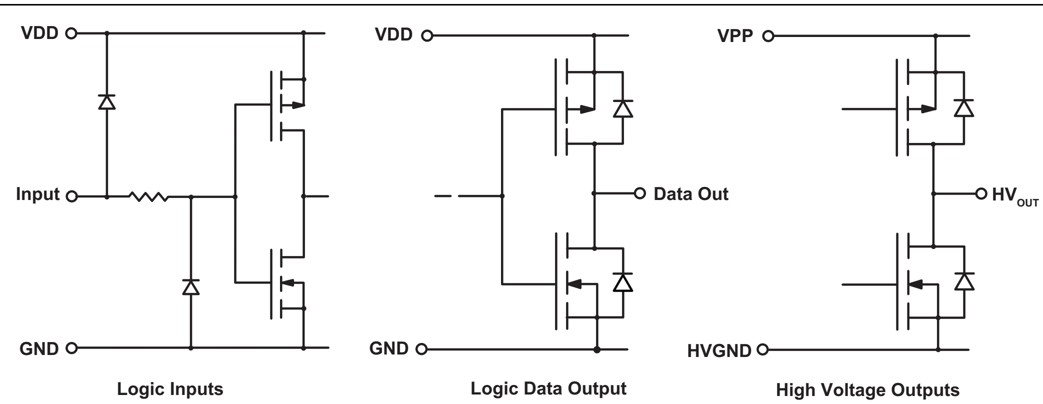
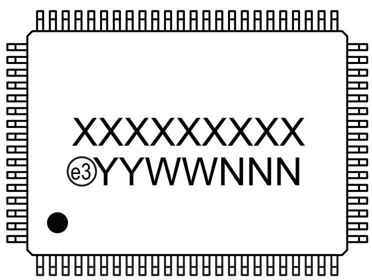


FIGURE 3-1: *Input and Output Equivalent Circuits.*

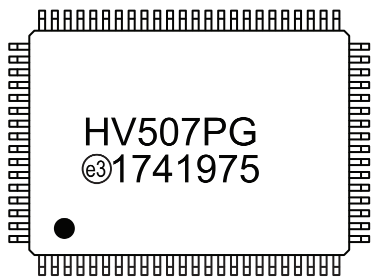
4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

80-lead PQFP



Example

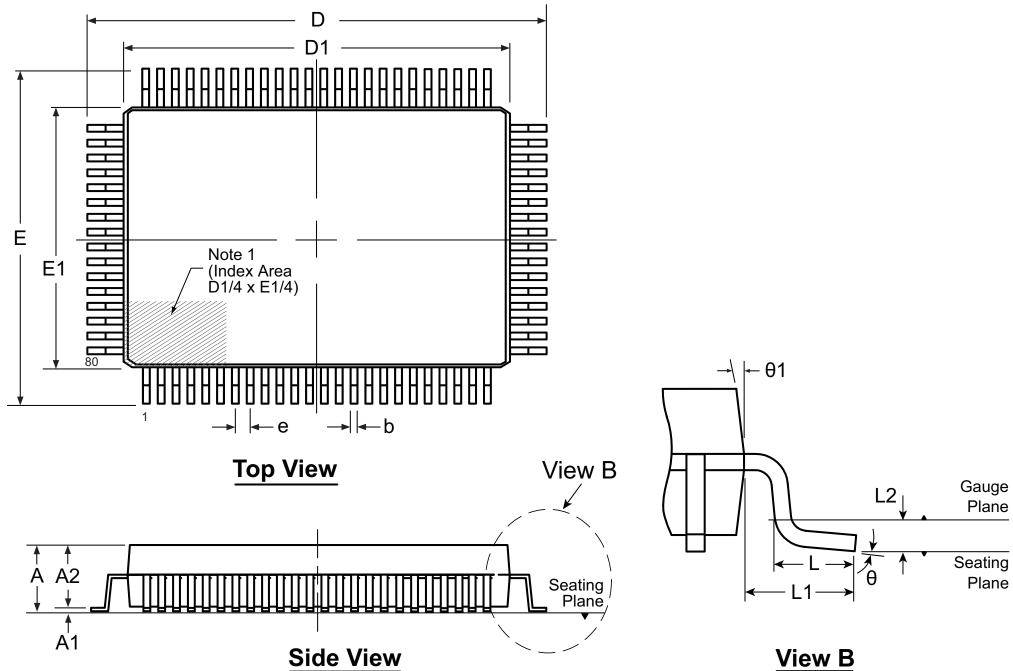


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

80-Lead PQFP Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc # DSFP-HV507 to Microchip DS20005845A
- Removed “Processed with HVCMOS® Technology” in the Features section
- Changed the package marking format
- Changed the quantity of the 80-lead PQFP PG package from 1000/Reel to 66/Tray
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV507	=	64-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs
Package:	PG	=	80-lead PQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a PG Package

Example:

a) HV507PG-G: 64-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, 80-lead PQFP, 66/Tray

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