HV264

Quad High-Voltage Amplifier Array

Features

- Four Independent High-voltage Amplifiers
- 190V Output Swing
- 9V/µs Typical Output Slew Rate
- 66.7V/V Fixed Gain
- High-value Internal Feedback Resistors
- Very Low Operating Current

Applications

- Tunable Laser
- Microelectromechanical Systems (MEMS) Driver
- Test Equipment
- Piezoelectric Transducer Driver
- Braille Driver

General Description

The HV264 is a quad high-voltage amplifier array integrated circuit. It operates on a 200V high-voltage supply and a 5V low-voltage supply. Each channel has its own input and output.

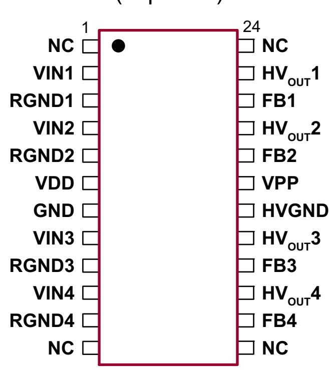
When both V_{OUT} and FB pins are connected together and RGND is set at 0V, a non-inverting amplifier is formed with a closed-loop gain of 66.7V/V. High-value internal feedback resistors are used to minimize power dissipation. The input voltage V_{IN} is designed for a range of 0.05V to 2.85V. The output can swing from 1V to V_{PP}–10V. A 2.85V input will cause the output to swing to 190V.

The HV264 is designed for maximum performance with minimal high-voltage current. The high-voltage current for each channel is less than 75 µA. The typical output slew rate performance is 9V/µs.

Package Type

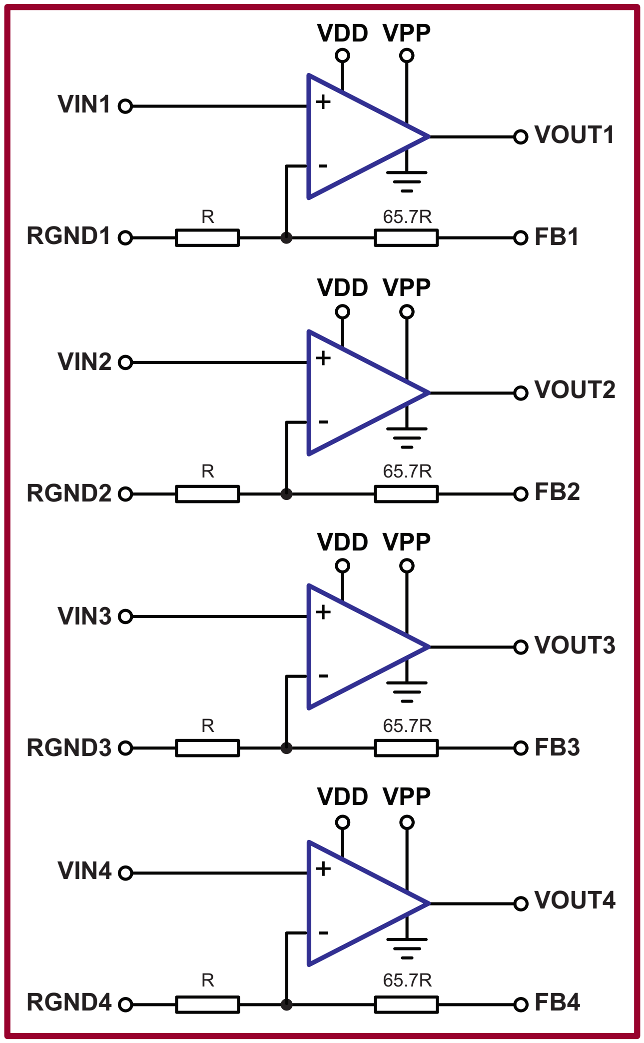
24-lead TSSOP

(Top view)

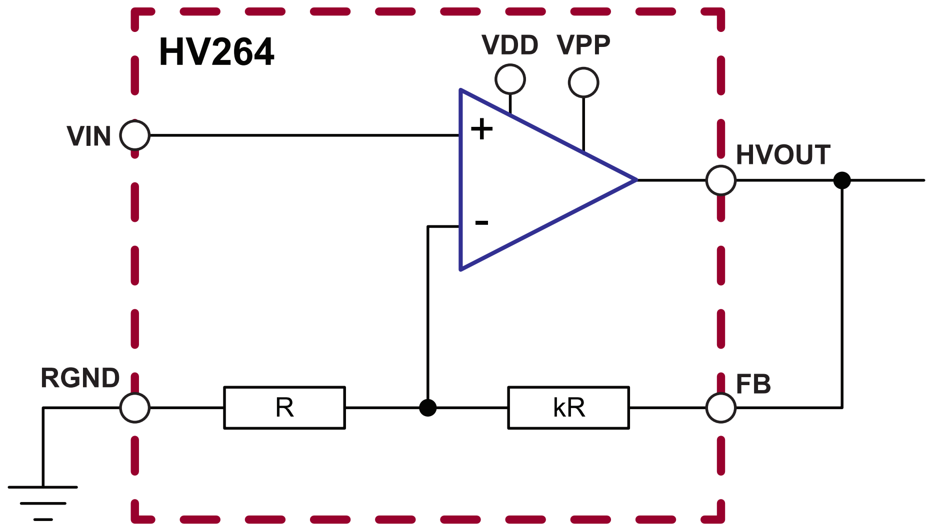


See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

High-voltage Supply, V_{PP} 225V
Low-voltage Supply, V_{DD} 6.5V
Output Voltage, HV_{OUT} .... 0V to V_{PP}
Analog Input Signal, V_{IN} .... 0V to V_{DD}
Maximum Junction Temperature, T_J .... 150°C
Storage Temperature, T_S .... –65°C to +150°C
ESD Rating (Note 1) .... ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Device is ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
High-voltage Positive Supply	V_{PP}	50	—	200	V	
Low-voltage Positive Supply	V_{DD}	4.5	5	5.5	V	
Input Ground Range	R_{GND}	0	0	V_{DD}	V	
V_{PP} Supply Current	I_{PP}	—	—	300	µA	V_{PP} = 200V, all inputs at 0V
V_{DD} Supply Current	I_{DD}	—	—	5	mA	V_{DD} = 5.5V
Operating Ambient Temperature	T_A	–40	—	85	°C	
Operating Junction Temperature	T_J	–40	—	100	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted, T_J = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
HV_{OUT} Voltage Swing	HV_{OUT}	1	—	V_{PP}–10	V	No load
HV_{OUT} Sink Current	I_{SINK}	3	—	—	mA	
HV_{OUT} Source Current	I_{SOURCE}	3	—	—	mA	
Input Voltage Range	V_{IN}	0	—	V_{DD}–1.5	V	
V_{IN} Input Current	I_{IN}	—	—	50	nA	
H_{VOUT} DC Offset	HV_{OS}	—	—	±1	V	V_{IN} = 0.2V

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted, T_J = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
HV_{OUT} Slew Rate–Rising Edge	SR	5	9	30	V/µs	V_{PP} = 200V, Load = 15 pF, measured between 10% to 90% of HV_{OUT}
HV_{OUT} Slew Rate–Falling Edge		—	9	—	V/µs	
Feedback Impedance, $R_f + R_i$	R_{FB}	3.5	5.3	—	MΩ	
Closed-loop Gain	A_V	63.4	66.7	70	V/V	
HV_{OUT} –3 dB Channel Bandwidth	BW	25	—	—	kHz	V_{PP} = 200V, Load = 15 pF
HV_{OUT} Capacitive Load	C_{LOAD}	0	—	15	pF	
Output Referred Noise	V_N	—	—	10	mV_{RMS}	Measured at HV_{OUT}, 0 kHz to 1 kHz single pole, V_{IN} = 0.2V
V_{DD} Power Supply Rejection Ratio	PSRR1	55	—	—	dB	V_{DD} = 4.5V to 5.5V V_{PP} = 200V, V_{IN} = 0.1V
V_{PP} Power Supply Rejection Ratio	PSRR2	60	—	—	dB	V_{DD} = 5V, V_{PP} = 50V to 200V, V_{IN} = 0.1V
Crosstalk	Xtalk	—	—	–80	dB	Output referred

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	85	°C	
Operating Junction Temperature	T_J	–40	—	100	°C	
Storage Temperature	T_S	–65	—	150	°C	
PACKAGE THERMAL RESISTANCE						
24-lead TSSOP	θ_{JA}	—	72	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

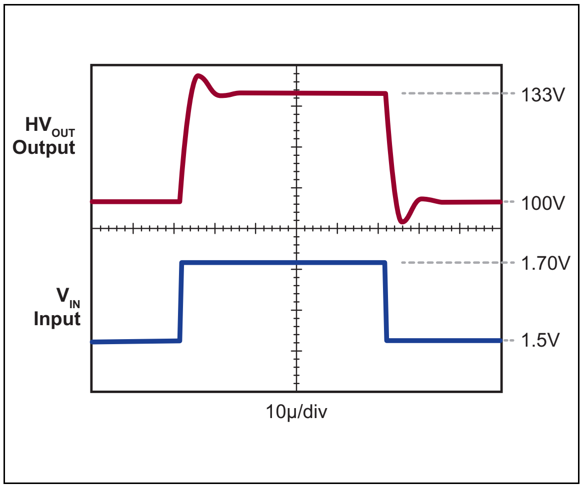


FIGURE 2-1: *Typical Small-signal Pulse Response.*

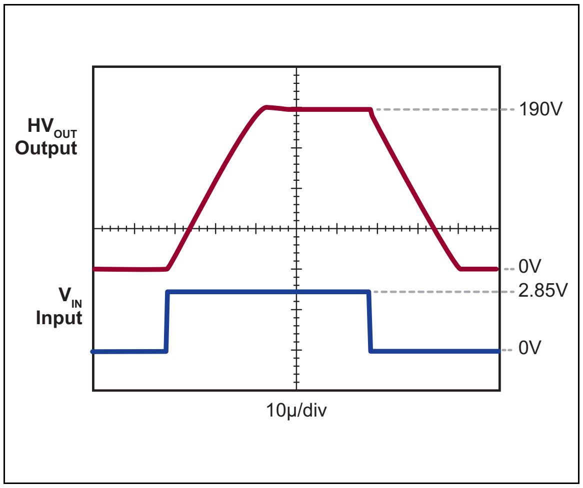


FIGURE 2-2: *Typical Large-signal Pulse Response.*

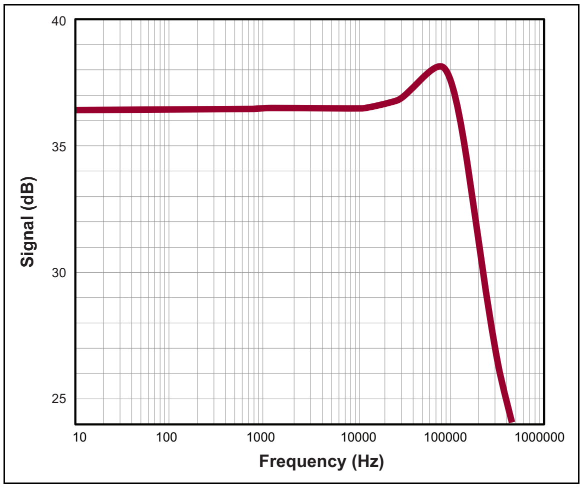


FIGURE 2-3: *Typical Bode Plot of Small-signal Gain (V_{IN} = 0.2 V_{P-P}, V_{DC} = 1.5V, V_{DD} = 5V and V_{PP} = 200V).*

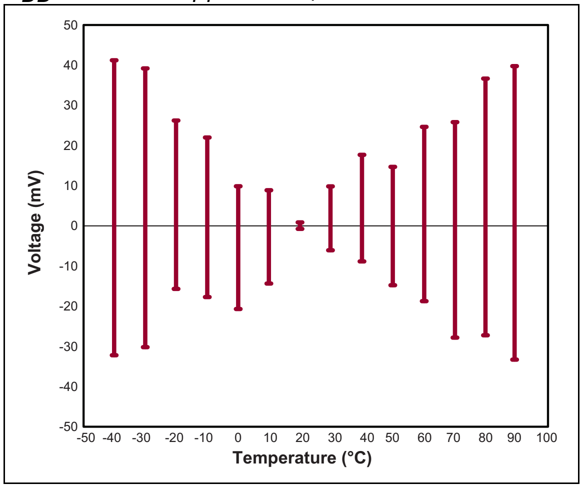


FIGURE 2-4: *Distribution of Typical HV_{OUT} Deviation over Temperature (V_{IN} = 0.1 V_{DC}, 1.6 V_{DC}, 3.3 V_{DC}, in reference to 20°C).*

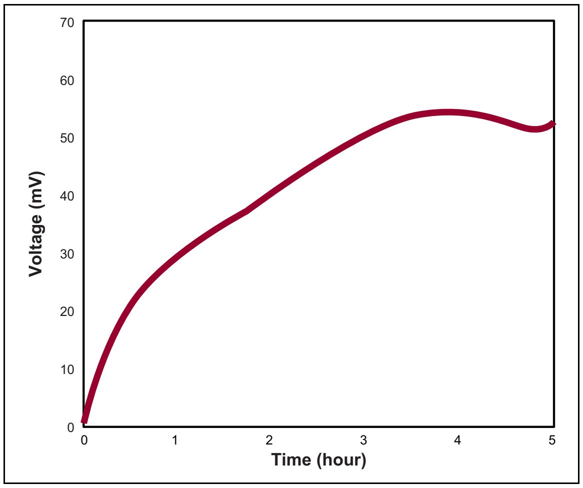


FIGURE 2-5: *Typical HV_{OUT} Drift Over Time (V_{PP} = 200V, V_{DD} = 5.5V, V_{IN} = 0.2V, Room Temperature and 50 pF Output Loading).*

3.0 PIN DESCRIPTION

The details on the pins of HV264 are listed on Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	No connection
2	VIN1	Amplifier Input 1
3	RGND1	Resistor ground for Channel 1. Typically grounded. Can be connected to a voltage source to create a DC offset.
4	VIN2	Amplifier Input 2
5	RGND2	Resistor ground for Channel 2. Typically grounded. Can be connected to a voltage source to create a DC offset.
6	VDD	Low-voltage positive supply
7	GND	Device ground
8	VIN3	Amplifier Input 3
9	RGND3	Resistor ground for Channel 3. Typically grounded. Can be connected to a voltage source to create a DC offset.
10	VIN4	Amplifier Input 4
11	RGND4	Resistor ground for Channel 4. Typically grounded. Can be connected to a voltage source to create a DC offset.
12	NC	No connection
13	NC	No connection
14	FB4	Feedback Input 4
15	HVOUT4	Amplifier Output 4
16	FB3	Feedback Input 3
17	HVOUT3	Amplifier Output 3
18	HVGND	Device high-voltage supply ground
19	VPP	High-voltage positive supply
20	FB2	Feedback Input 2
21	HVOUT2	Amplifier Output 2
22	FB1	Feedback Input 1
23	HVOUT1	Amplifier Output 1
24	NC	No connection

4.0 FUNCTIONAL DESCRIPTION

4.1 Power-up/Power-down Sequence

The device can be damaged due to improper power-up/power-down sequence. To avoid this, please follow the acceptable power-up and power-down sequences in Table 4-1 and Table 4-2 and add an external diode across V_{PP} and V_{DD} where the anode of the diode is connected to V_{DD} and the cathode of the diode is connected to V_{PP}. Any low-current high-voltage diode such as a 1N4004 will be adequate.

TABLE 4-1: ACCEPTABLE POWER-UP SEQUENCES

Option 1		Option 2	
Step	**Description**	**Step**	**Description**
1	V_{DD}	1	V_{DD}
2	V_{PP}	2	Inputs
3	Inputs	3	V_{PP}

TABLE 4-2: ACCEPTABLE POWER-DOWN SEQUENCES

Option 1		Option 2	
Step	**Description**	**Step**	**Description**
1	Inputs	1	V_{PP}
2	V_{PP}	2	Inputs
3	V_{DD}	3	V_{DD}

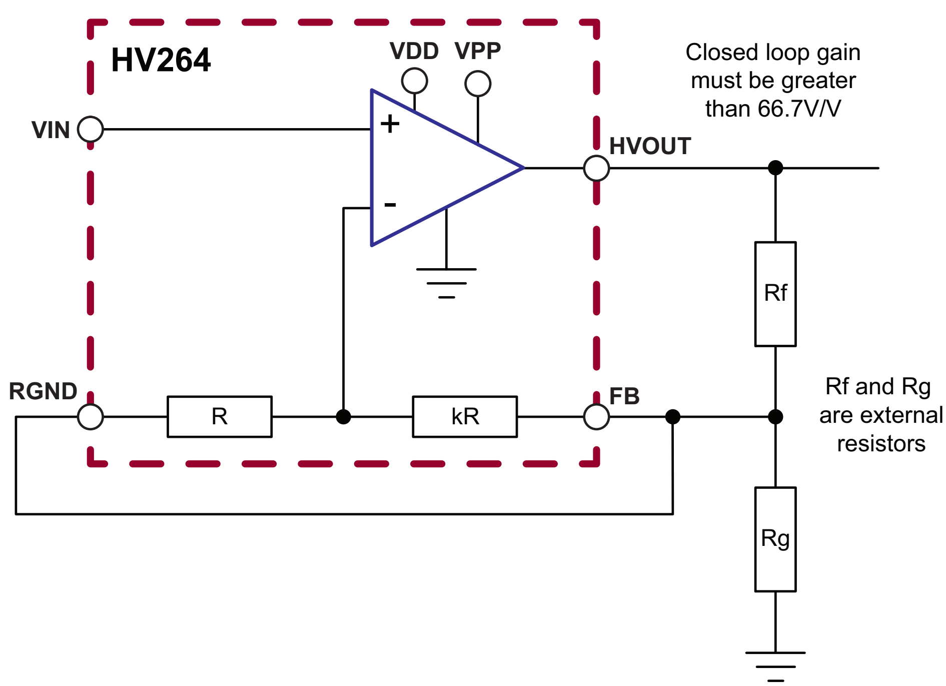
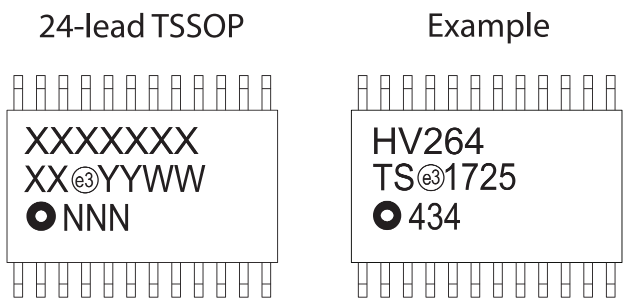


FIGURE 4-1: Application Circuit with External Gain Setting Resistors.

5.0 PACKAGE MARKING INFORMATION

5.1 Packaging Information

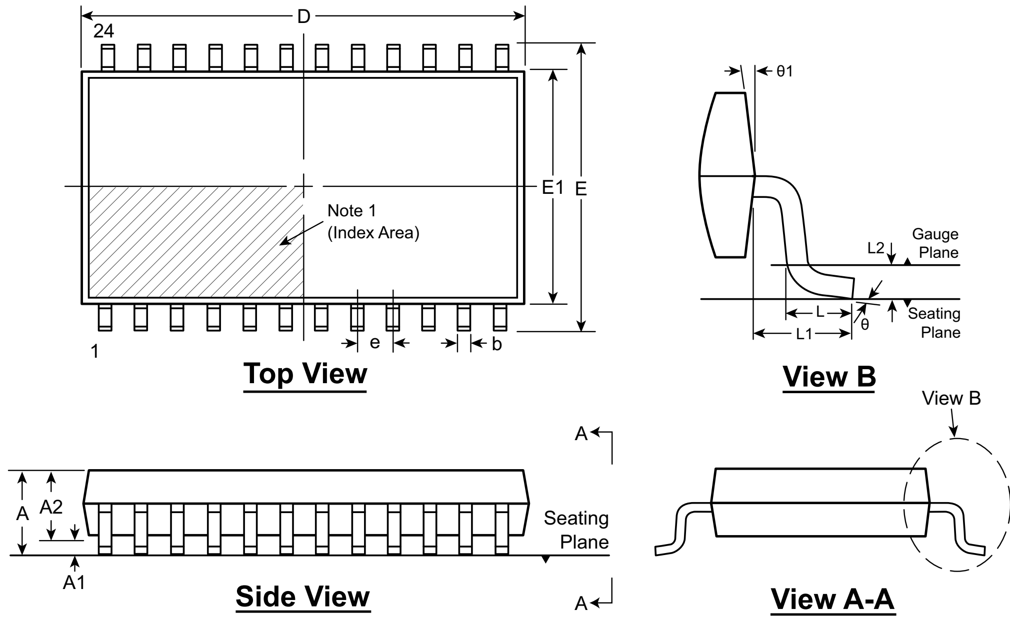


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

24-Lead TSSOP Package Outline (TS)

7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30		0.45			0°	
Dimension (mm)	NOM	-	-	1.00	-	7.80	6.40	4.40	0.65 BSC	0.60	1.00 REF	0.25 BSC	-	12° REF
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2017)

- Converted Supertex Doc# DSFP-HV264 to Microchip DS20005832A
- Changed the part marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV264	=	Quad High-Voltage Amplifier Array
Package:	TS	=	24-lead TSSOP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	2500/Reel for a TS Package

Example:

a) HV264TS-G: Quad High-Voltage Amplifier Array, 24-lead TSSOP, 2500/Reel

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