HV257

32-Channel High-Voltage Sample-and-Hold Amplifier Array

Features

- Thirty-two Independent High-voltage Amplifiers
- 300V Operating Voltage
- 295V Output Voltage
- 2.2V/µs Typical Output Slew Rate
- Adjustable Output Current Source Limit
- Adjustable Output Current Sink Limit
- Internal Closed-loop Gain of 72V/V
- 12 MΩ Feedback Impedance
- Layout Ideal for Die Applications

Applications

- Microelectromechanical Systems (MEMS) Driver
- Piezoelectric Transducer Driver
- Optical Crosspoint Switches (Using MEMS Technology)

General Description

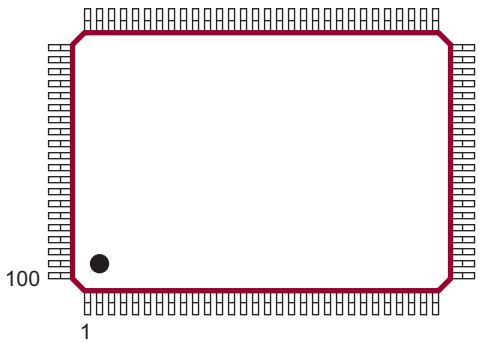
The HV257 is a 32-channel, high-voltage sample-and-hold amplifier array integrated circuit. It operates on a single high-voltage supply, up to 300V, and two low-voltage supplies, V_{DD} and V_{NN}.

All 32 sample-and-hold circuits share a common analog input, V_{SIG}. The individual sample-and-hold circuits are selected by a five-to-32 logic decoder. The sampled voltage on the holding capacitor is buffered by a low-voltage amplifier and is magnified by a high-voltage amplifier with a closed-loop gain of 72V/V. The internal closed-loop gain is set for an input voltage range of 0V to 4.096V. The input voltage can be up to 5V, but the output will saturate. The maximum output voltage swing is 5V below the V_{PP} high-voltage supply. The outputs can drive capacitive loads of up to 3000 pF.

The maximum output source and sink current can be adjusted by using two external resistors. An external R_{SOURCE} resistor controls the maximum sourcing current, and an external R_{SINK} resistor controls the maximum sinking current. The current limit is approximately 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low-voltage silicon junction diode is made available to help monitor the die temperature.

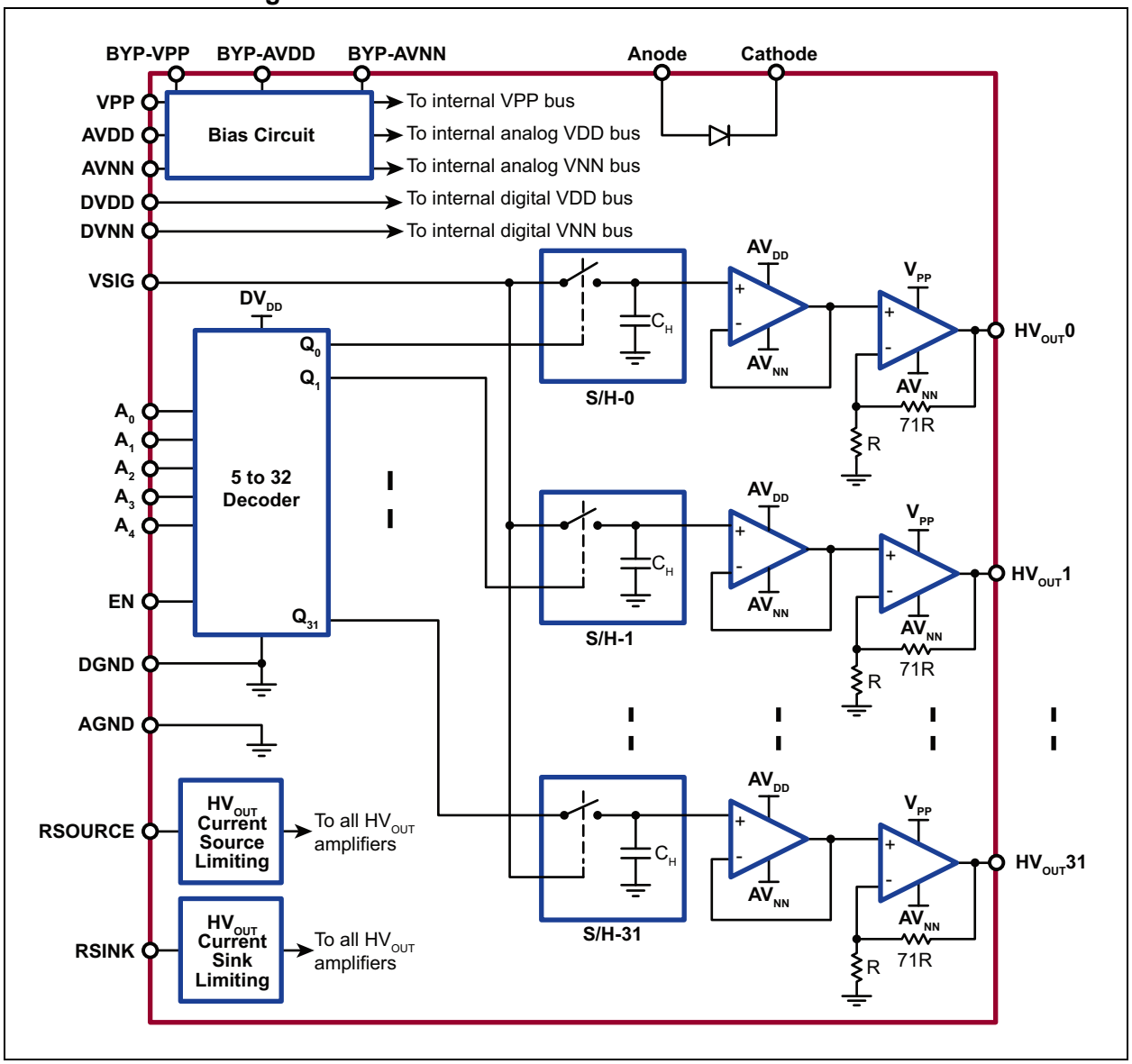
Package Type

100-lead MQFP
(Top view)

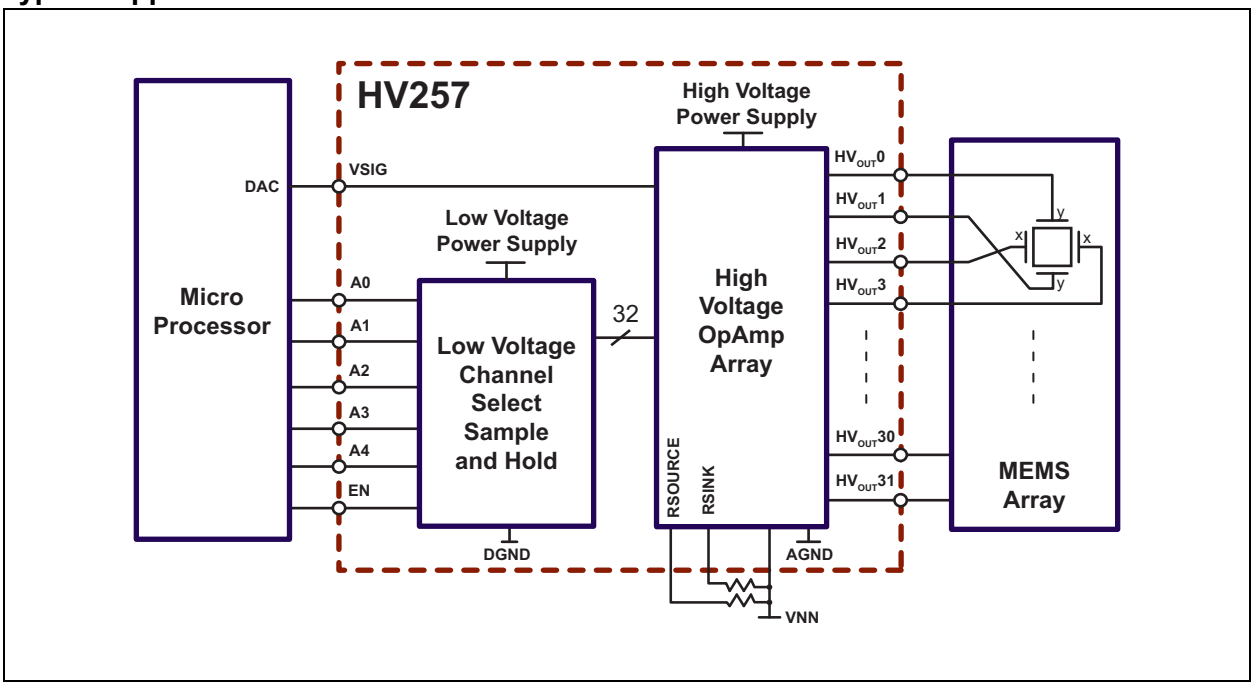


See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

High-voltage Supply, V_{PP} 310V
Analog Low-voltage Positive Supply, AV_{DD} 8V
Digital Low-voltage Positive Supply, DV_{DD} 8V
Analog Low-voltage Negative Supply, AV_{NN} ..... –7V
Digital Low-voltage Negative Supply, DV_{NN} ..... –7V
Logic Input Voltage ..... –0.5V to DV_{DD}
Analog Input Signal, V_{SIG} ..... 0V to 6V
Maximum Junction Temperature, T_J ..... 150°C
Storage Temperature, T_S ..... –65°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
High-voltage Positive Supply	V_{PP}	125	—	300	V	
Low-voltage Positive Supply	V_{DD}	6	—	7.5	V	
Low-voltage Negative Supply	V_{NN}	–4.5	—	–6.5	V	
V_{PP} Supply Current	I_{PP}	—	—	0.8	mA	V_{PP} = 300V, All HV_{OUT} = 0V, No load
V_{DD} Supply Current	I_{DD}	—	—	5	mA	V_{DD} = 6V to 7.5V
V_{NN} Supply Current	I_{NN}	–6	—	—	mA	V_{NN} = –4.5V to –6.5V
Operating Temperature Range	T_J	–10	—	85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
HV_{OUT} Voltage Swing	HV_{OUT}	0	—	V_{PP}–5	V	
Input Voltage Offset	V_{INOS}	—	—	±40	mV	Input referred
Feedback Resistance from HV_{OUT} to Ground	R_{FB}	9.6	12	—	MΩ	
HV_{OUT} Capacitive Load	C_{LOAD}	0	—	3000	pF	
HV_{OUT} Sourcing Current Limiting Range	I_{SOURCE}	50	—	500	µA	I_{SOURCE} = 12.5V/R_{SOURCE}
HV_{OUT} Sinking Current Limiting Range	I_{SINK}	50	—	500	µA	I_{SINK} = 12.5V/R_{SINK}
External Resistance Range for Setting Maximum Current Source	R_{SOURCE}	25	—	250	kΩ	
External Resistance Range for Setting Maximum Current Sink	R_{SINK}	25	—	250	kΩ	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
HV_{OUT} Slew Rate Rise	SR	—	2.2	—	V/µs	No load
HV_{OUT} Slew Rate Fall		—	2	—	V/µs	No load
HV_{OUT} –3 dB Channel Bandwidth	BW	—	4	—	kHz	V_{PP} = 300V
Open-loop Gain	A_O	70	100	—	dB	
Closed-loop Gain	A_V	68.4	72	75.6	V/V	
DC Channel-to-channel Crosstalk	CT_{DC}	–80	—	—	dB	
Power Supply Rejection Ratio for V_{PP}, V_{DD} and V_{NN}	PSRR	–40	—	—	dB	
SAMPLE AND HOLD						
Acquisition Time	t_{AQ}	—	4	—	µs	
Pedestal Voltage	V_{PED}	—	1	—	mV	Input referred
Sample-and-Hold Switch Resistance	R_{SW}	—	5	—	kΩ	
Sample-and-Hold Capacitor	C_H	—	10	12	pF	
Voltage Droop Rate During Hold Time Relative to Input	V_{DROOP}	—	6	—	V/s	Output referred
Input Signal Voltage Range	V_{SIG}	0	—	5	V	
V_{SIG} Input Capacitance	C_{SIG}	—	33	—	pF	
LOGIC DECODER						
Set-up Time-address to Enable	t_{SU}	75	—	—	ns	
Hold Time-address to Enable Bar	t_H	75	—	—	ns	
Input Logic High Voltage	V_{IH}	2.4	—	V_{DD}	V	
Input Logic Low Voltage	V_{IL}	0	—	1.2	V	
Input Logic High Current	I_{IH}	—	—	1	µA	V_{IH} = V_{DD}
Input Logic Low Current	I_{IL}	–1	—	—	µA	V_{IL} = 0V
Logic Input Capacitance	C_{IN}	—	—	15	pF	

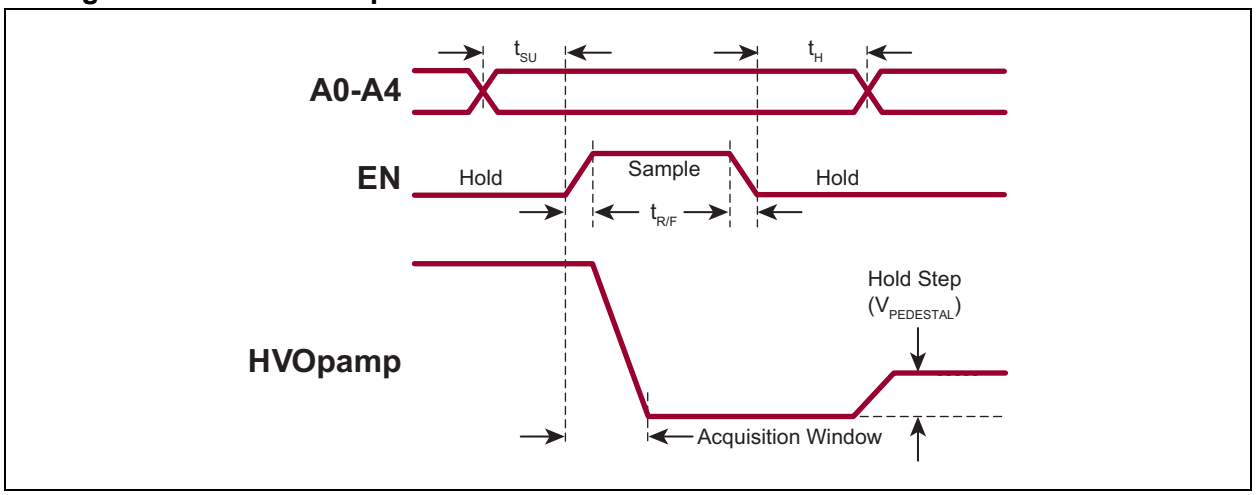
AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over operating conditions unless otherwise noted						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE DIODE						
Peak Inverse Voltage	PIV	—	—	5	V	Cathode to anode
Forward Diode Drop	V_F	—	0.6	—	V	I_F = 100 µA, anode to cathode at T_A = 25°C
Forward Diode Current	I_F	—	—	100	µA	Anode to cathode
V_F Temperature Coefficient	T_C	—	–2.2	—	mV/°C	Anode to cathode

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
100-lead MQFP	θ_{JA}	—	39	—	°C/W	

Timing Waveforms of Sample-and-Hold



DECODER FUNCTION TABLE

A_4	A_3	A_2	A_1	A_0	EN	Selected S/H
L	L	L	L	L	H	0
L	L	L	L	H	H	1
L	L	L	H	L	H	2
L	L	L	H	H	H	3
↕	↕	↕	↕	↕	↕	↕
H	H	H	H	L	H	30
H	H	H	H	H	H	31
X	X	X	X	X	L	All Open

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

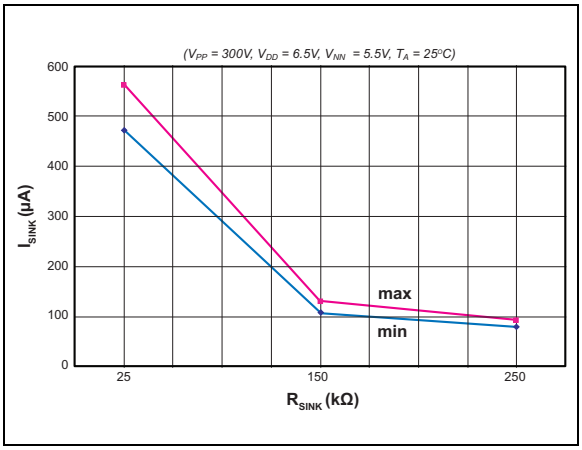


FIGURE 2-1: *I_{SINK} vs. R_{SINK}.*

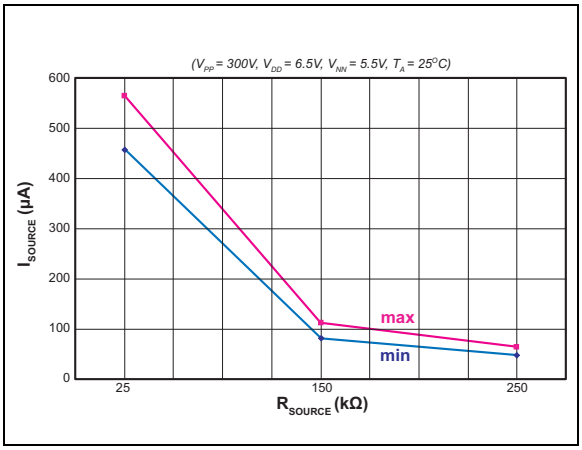


FIGURE 2-2: *I_{SOURCE} vs. R_{SOURCE}.*

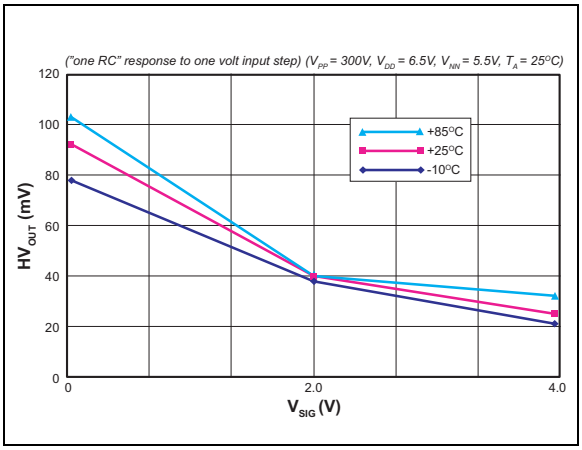


FIGURE 2-3: *Acquisition Window.*

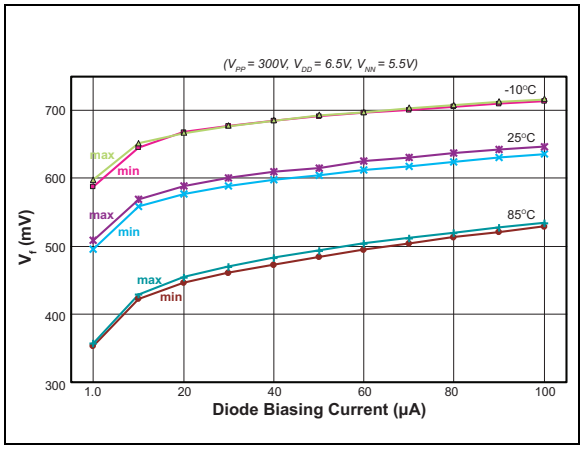


FIGURE 2-4: *Temperature Diode vs. Temperature.*

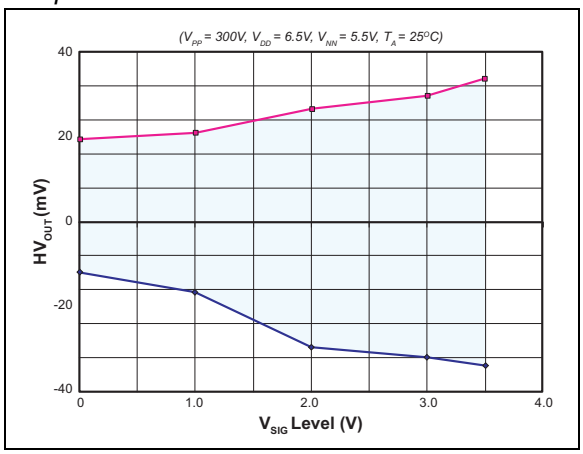


FIGURE 2-5: *HV_{OUT} Charge Injection vs. V_{SIG}*

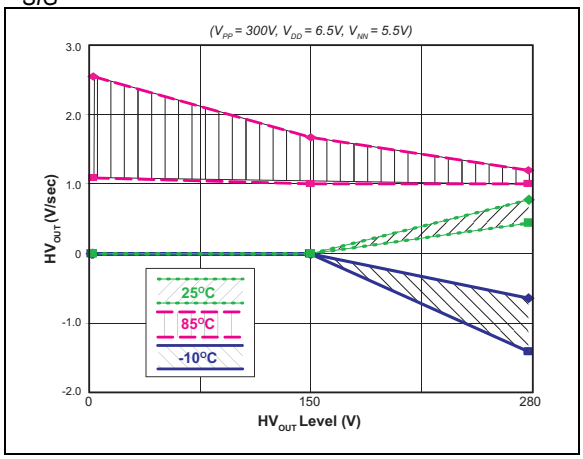


FIGURE 2-6: *H_{VOUT} Droop.*

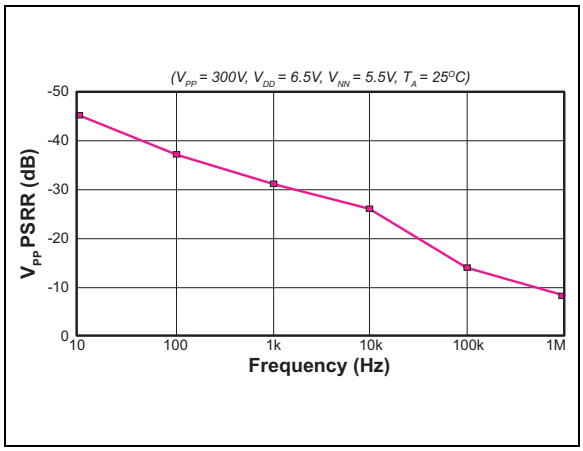


FIGURE 2-7: *V_{PP} PSRR vs. Frequency.*

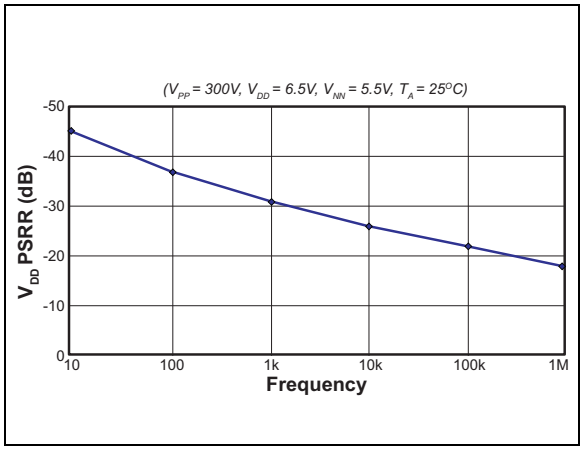


FIGURE 2-8: *V_{DD} PSRR vs. Frequency.*

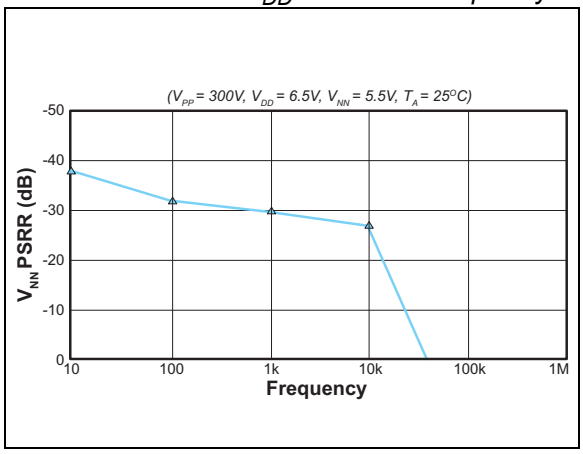


FIGURE 2-9: *V_{NN} PSRR vs. Frequency.*

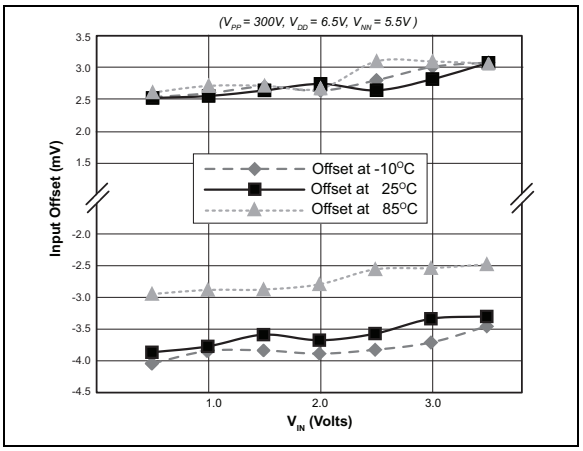


FIGURE 2-10: *Input Offset vs. V_{IN} and Temperature.*

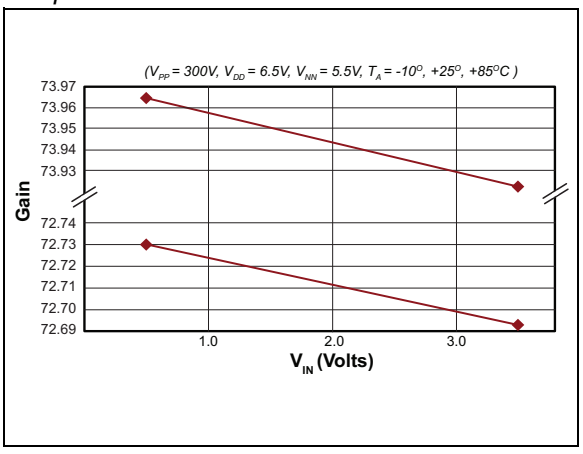


FIGURE 2-11: *Gain vs. V_{IN}.*

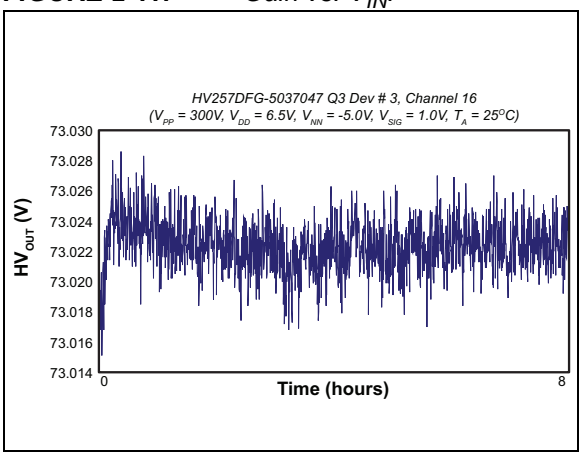


FIGURE 2-12: *HV_{OUT} Drift.*

3.0 PIN DESCRIPTION

The details on the pins of HV257 are listed on Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT31	Amplifier output
2	HVOUT30	Amplifier output
3	HVOUT29	Amplifier output
4	HVOUT28	Amplifier output
5	HVOUT27	Amplifier output
6	HVOUT26	Amplifier output
7	HVOUT25	Amplifier output
8	HVOUT24	Amplifier output
9	HVOUT23	Amplifier output
10	HVOUT22	Amplifier output
11	HVOUT21	Amplifier output
12	HVOUT20	Amplifier output
13	HVOUT19	Amplifier output
14	HVOUT18	Amplifier output
15	HVOUT17	Amplifier output
16	HVOUT16	Amplifier output
17	HVOUT15	Amplifier output
18	HVOUT14	Amplifier output
19	HVOUT13	Amplifier output
20	HVOUT12	Amplifier output
21	HVOUT11	Amplifier output
22	HVOUT10	Amplifier output
23	HVOUT9	Amplifier output
24	HVOUT8	Amplifier output
25	HVOUT7	Amplifier output
26	HVOUT6	Amplifier output
27	HVOUT5	Amplifier output
28	HVOUT4	Amplifier output
29	HVOUT3	Amplifier output
30	HVOUT2	Amplifier output
31	HVOUT1	Amplifier output
32	HVOUT0	Amplifier output
33	VPP	High-voltage positive supply. There are two pads.
34	NC	No connection
35	NC	No connection

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	AGND	Analog ground. There are three pads. They need to be externally connected.
40	AVNN	Analog low-voltage negative supply. This should be at the same potential as DVNN. There are two pads.
41	NC	No connection
42	AVDD	Analog low-voltage positive supply. This should be at the same potential as DVDD. There are two pads.
43	AGND	Analog ground. There are three pads. They need to be externally connected.
44	DVNN	Digital low-voltage negative supply. This should be at the same potential as AVNN. There are two pads.
45	DVDD	Digital low-voltage positive supply. This should be at the same potential as AVDD. There are two pads.
46	NC	No connection
47	NC	No connection
48	NC	No connection
49	NC	No connection
50	NC	No connection
51	NC	No connection
52	NC	No connection
53	NC	No connection
54	NC	No connection
55	NC	No connection
56	NC	No connection
57	NC	No connection
58	NC	No connection
59	NC	No connection
60	NC	No connection
61	NC	No connection
62	NC	No connection
63	NC	No connection
64	NC	No connection
65	NC	No connection
66	NC	No connection
67	NC	No connection
68	NC	No connection
69	NC	No connection
70	NC	No connection
71	NC	No connection

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
72	NC	No connection
73	NC	No connection
74	NC	No connection
75	NC	No connection
76	NC	No connection
77	NC	No connection
78	NC	No connection
79	NC	No connection
80	EN	Active logic high input. Logic low will keep sample-and-hold switches open.
81	A0	Decoder logic input. Addressed channel will close the sample-and-hold switch. Sample-and-hold switches for unaddressed channels are kept open.
82	A1	Decoder logic input. Addressed channel will close the sample-and-hold switch. Sample-and-hold switches for unaddressed channels are kept open.
83	A2	Decoder logic input. Addressed channel will close the sample-and-hold switch. Sample-and-hold switches for unaddressed channels are kept open.
84	A3	Decoder logic input. Addressed channel will close the sample-and-hold switch. Sample-and-hold switches for unaddressed channels are kept open.
85	A4	Decoder logic input. Addressed channel will close the sample-and-hold switch. Sample-and-hold switches for unaddressed channels are kept open.
86	DGND	Digital ground
87	DVDD	Digital low-voltage positive supply. This should be at the same potential as AVDD. There are two pads.
88	DVNN	Digital low-voltage negative supply. This should be at the same potential as AVNN. There are two pads.
89	AGND	Analog ground. There are three pads. They need to be externally connected.
90	VSIG	Common input signal for all 32 sample-and-hold circuits.
91	AVDD	Analog low-voltage positive supply. This should be at the same potential as DVDD. There are two pads.
92	BYP-AVNN	Internally generated reference voltage. An external low-voltage (1 nF–10 nF) capacitor needs to be connected across AVNN and BYP-AVNN.
93	BYP-AVDD	Internally generated reference voltage. An external low-voltage (1 nF–10 nF) capacitor needs to be connected across AVDD and BYP-AVDD.
94	AVNN	Analog low-voltage negative supply. This should be at the same potential as DVNN. There are two pads.
95	Anode	The anode side of a low-voltage silicon diode that can be used to monitor die temperature.
96	Cathode	The cathode side of a low-voltage silicon diode that can be used to monitor die temperature.
97	RSINK	The external resistor from RSINK to VNN that sets the output current sinking limit. The current limit is approximately 12.5V divided by the RSINK resistor value.
98	RSOURCE	The external resistor from RSOURCE to VNN that sets the output current sourcing limit. The current limit is approximately 12.5V divided by RSOURCE resistor value.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
99	BYP-VPP	The internally generated reference voltage. An external low-voltage (1 nF–10 nF) capacitor needs to be connected across VPP and BYP-VPP.
100	VPP	High-voltage positive supply. There are two pads.

3.1 Pad Configuration

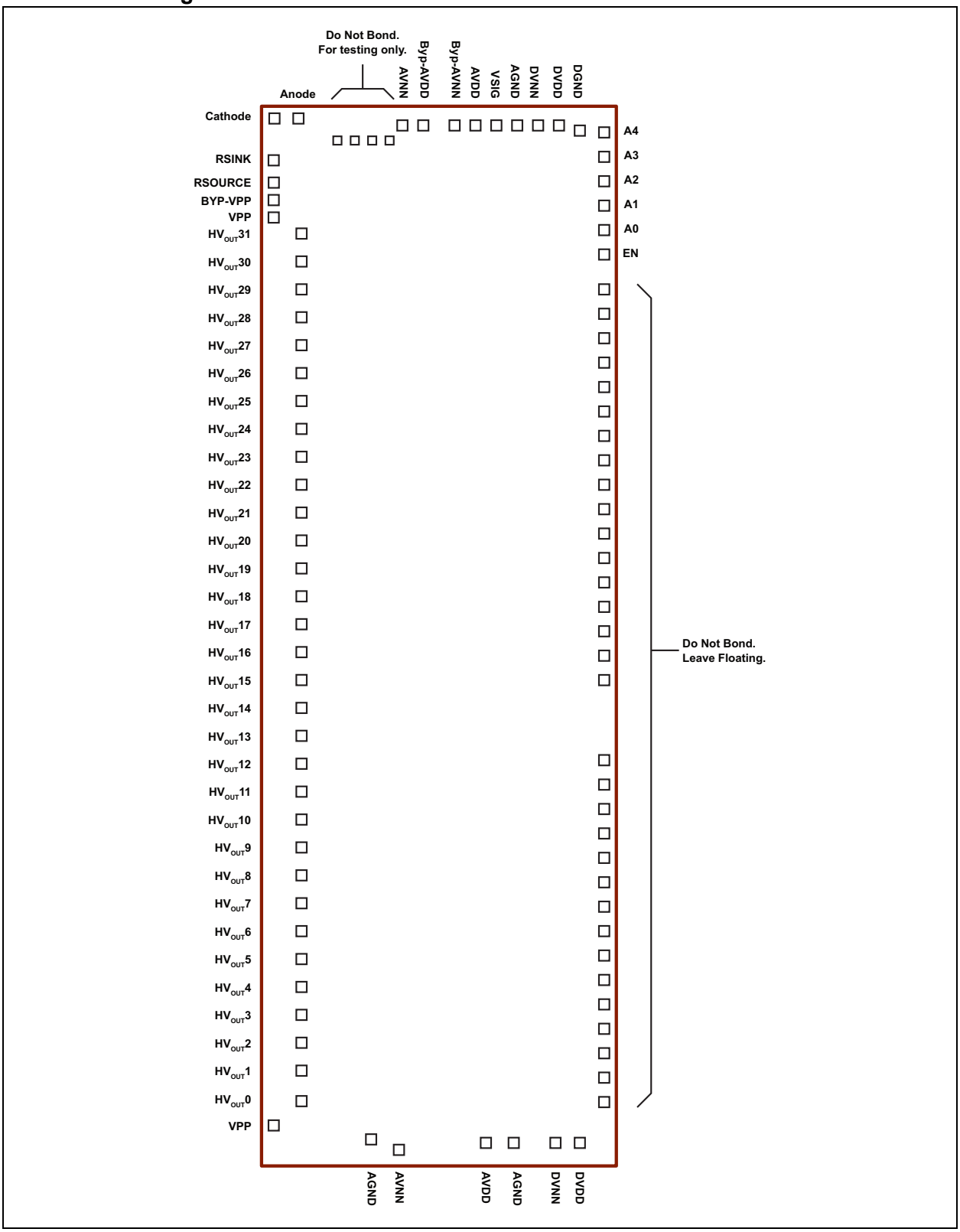


FIGURE 3-1: *Pad Configuration Drawing.*

TABLE 3-2: PAD COORDINATES

Chip Size: 17160 µm X 5830 µm **Center of Die:** 0,0		
Pad Name	**X (µm)**	**Y (µm)**
VPP	–8338.5	2708.5
HVOUT0	–7895	2305.5
HVOUT1	–7448.5	2305.5
HVOUT2	–7001.5	2305.5
HVOUT3	–6554.5	2305.5
HVOUT4	–6107.5	2305.5
HVOUT5	–5660.5	2305.5
HVOUT6	–5213.5	2305.5
HVOUT7	–4776.5	2305.5
HVOUT8	–4319.5	2305.5
HVOUT9	–3872.5	2305.5
HVOUT10	–3425.5	2305.5
HVOUT11	–2978.5	2305.5
HVOUT12	–2513.5	2305.5
HVOUT13	–2084.5	2305.5
HVOUT14	–1637.5	2305.5
HVOUT15	–1190.5	2305.5
HVOUT16	–743.5	2305.5
HVOUT17	–296.5	2305.5
HVOUT18	150	2305.5
HVOUT19	597.5	2305.5
HVOUT20	1044.5	2305.5
HVOUT21	1491.5	2305.5
HVOUT22	1938.5	2305.5
HVOUT23	2385.5	2305.5
HVOUT24	2832.5	2305.5
HVOUT25	3279.5	2305.5
HVOUT26	3726.5	2305.5
HVOUT27	4173.5	2305.5
HVOUT28	4620.5	2305.5
HVOUT29	5067.5	2305.5
HVOUT30	5514.5	2305.5
HVOUT31	5961.5	2305.5
VPP	6659	2709
BYP-VPP	7045	2709
RSOURCE	7489	2709
RSINK	7969	2709
CATHODE	8366	2709
ANODE	8366	2199
AVNN	8047	425
BYP-AVDD	8047	125.5

TABLE 3-2: PAD COORDINATES (CONTINUED)

Chip Size: 17160 µm X 5830 µm **Center of Die:** 0,0		
Pad Name	**X (µm)**	**Y (µm)**
BYP-AVNN	8047	–135.5
AVDD	8047	–704.5
VSIG	8047	–1072.5
AGND	8047	–1424.5
DVNN	8066.5	–1590
DVDD	8066.5	–1958.5
DGND	7867	–2192
A4	7723	–2684
A3	7319	–2684
A2	6913	–2684
A1	6508.5	–2684
A0	6103.5	–2684
EN	5698	–2684
NC	5043.5	–2686
NC	4638.5	–2686
NC	4233.5	–2686
NC	3828.5	–2686
NC	3423.5	–2686
NC	3018.5	–2686
NC	2613.5	–2686
NC	2208.5	–2686
NC	1803.5	–2686
NC	1398.5	–2686
NC	993.5	–2686
NC	588.5	–2686
NC	183.5	–2686
NC	–221.5	–2686
NC	–626.5	–2686
NC	–1031.5	–2686
NC	–1436.5	–2686
NC	–2412	–2686
NC	–2817	–2686
NC	–3222	–2686
NC	–3627	–2686
NC	–4032	–2686
NC	–4437	–2686
NC	–4842	–2686
NC	–5247	–2686
NC	–5652	–2686
NC	–6052	–2686
NC	–6462	–2686

TABLE 3-2: PAD COORDINATES (CONTINUED)

Chip Size: 17160 µm X 5830 µm **Center of Die:** 0,0		
Pad Name	**X (µm)**	**Y (µm)**
NC	–6867	–2686
NC	–7272	–2686
NC	–7677	–2686
NC	–8082	–2686
DVDD	–8373	–2250.5
DVNN	–8373	–1949
AGND	–8367	–1561
AVDD	–8387	–1143
AVNN	–8338.5	577.5
AGND	–8341	916.5

4.0 FUNCTIONAL DESCRIPTION

4.1 Power-up/Power-down Sequence

4.1.1 EXTERNAL DIODE PROTECTION

The device can be damaged due to improper power-up/power-down sequence. To avoid this, please follow the acceptable power-up/power-down sequences in Table 4-1 and Table 4-2 and add two external diodes as shown in Figure 4-1. The first diode is a high-voltage diode across V_{PP} and V_{DD} where the anode of the diode is connected to V_{DD} and the cathode of the diode is connected to V_{PP}. Any low-current high-voltage diode such as a 1N4004 will be adequate. The second diode is a Schottky diode across V_{NN} and D_{GND} where the anode of the Schottky diode is connected to V_{NN} and the cathode is connected to D_{GND}. Any low-current Schottky diode such as a 1N5817 will be sufficient.

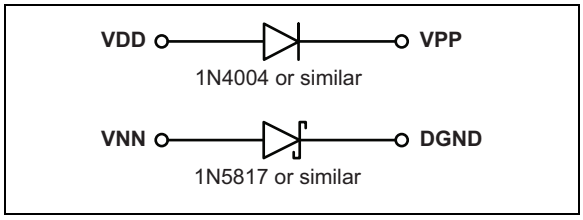


FIGURE 4-1: *Diode Configuration.*

4.1.2 RECOMMENDED POWER-UP/POWER-DOWN SEQUENCE

The HV257 needs all power supplies to be fully up and all channels refreshed with V_{SIG} = 0V to force all high-voltage outputs to 0V. Before that time, the high-voltage outputs may have temporary voltage excursions above or below GND level, depending on selected power-up sequence. To minimize the excursions, the V_{DD} and V_{NN} power supplies should be applied at the same time (or within a few nanoseconds). In addition, all channels should be continuously refreshed with V_{SIG} = 0V, just before, and while the V_{PP} is ramping up. The suggested V_{PP} ramp up speed should be 10 milliseconds or longer and the ramp-down should be 1 millisecond or longer.

TABLE 4-1: ACCEPTABLE POWER-UP SEQUENCES

Option 1		Option 2		Option 3	
Step	**Description**	**Step**	**Description**	**Step**	**Description**
1	V_{PP}	1	V_{NN}	1	V_{DD} and V_{NN}
2	V_{NN}	2	V_{DD}	2	Inputs
3	V_{DD}	3	V_{PP}	3	V_{PP}
4	Inputs and Anode	4	Inputs and Anode	4	Anode

TABLE 4-2: ACCEPTABLE POWER-DOWN SEQUENCES

Option 1		Option 2		Option 3	
Step	**Description**	**Step**	**Description**	**Step**	**Description**
1	Inputs and Anode	1	Inputs and Anode	1	Anode
2	V_{DD}	2	V_{PP}	2	V_{PP}
3	V_{NN}	3	V_{DD}	3	Inputs
4	V_{PP}	4	V_{NN}	4	V_{NN} and V_{DD}

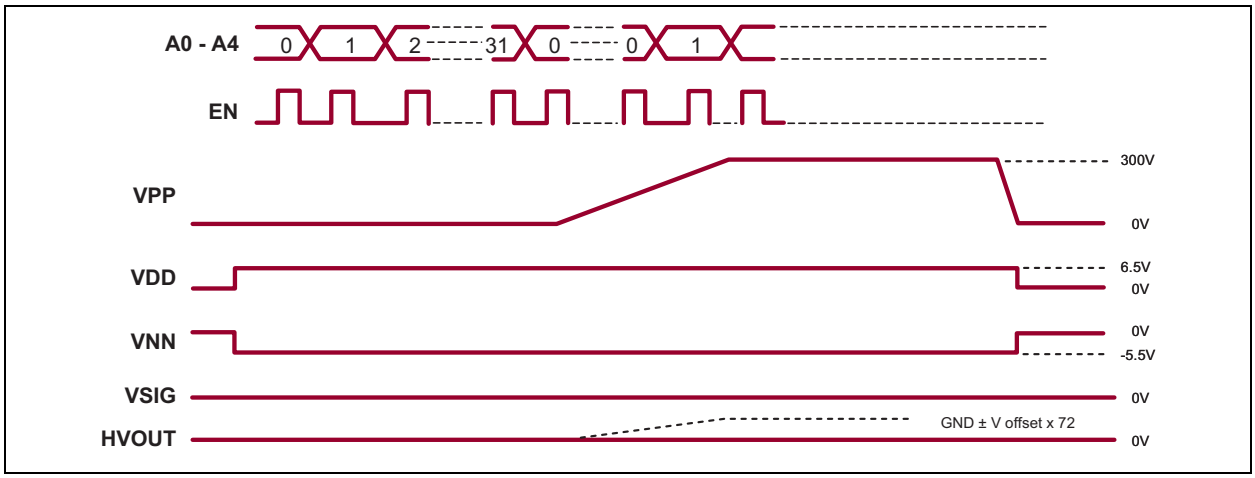


FIGURE 4-2: *Recommended Power-up/Power-down Timing.*

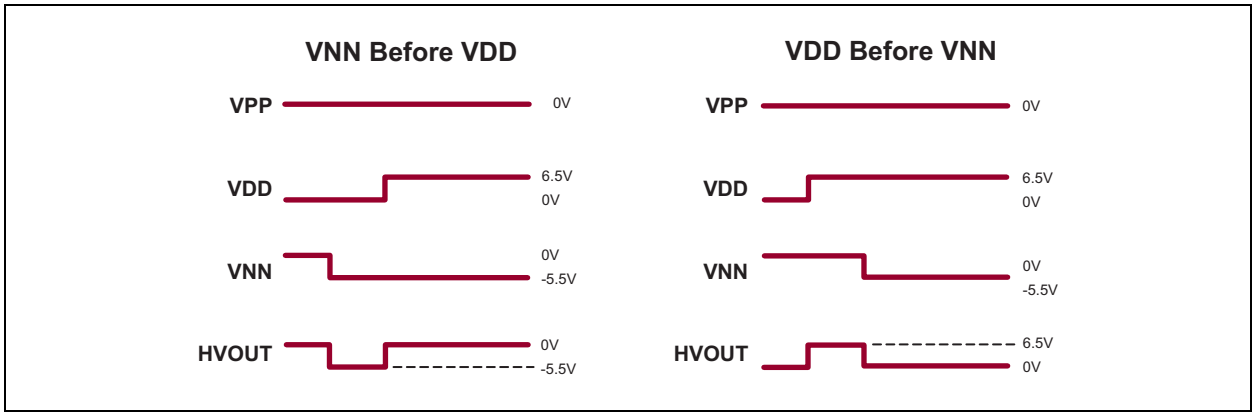


FIGURE 4-3: *HV_{OUT} Level at Power-up.*

4.2 R_{SINK}/R_{SOURCE}

The V_{DD}_BYP, V_{DD}_BYP and V_{NN}_BYP pins are internal high-impedance-current mirror gate nodes brought out to maintain stable opamp biasing currents in noisy power supply environments. When 0.1 µF/25V bypass capacitors are added between V_{PP}_BYP and V_{PP}, between V_{DD}_BYP and V_{DD} and between V_{NN}_BYP and V_{NN}, they will force the high-impedance gate nodes to follow the fluctuation of power lines. The expected voltages at the V_{DD}_BYP and V_{NN}_BYP pins are typically 1.5V from their respectful power supply. The expected voltage at V_{PP}_BYP is typically 3V below V_{PP}.

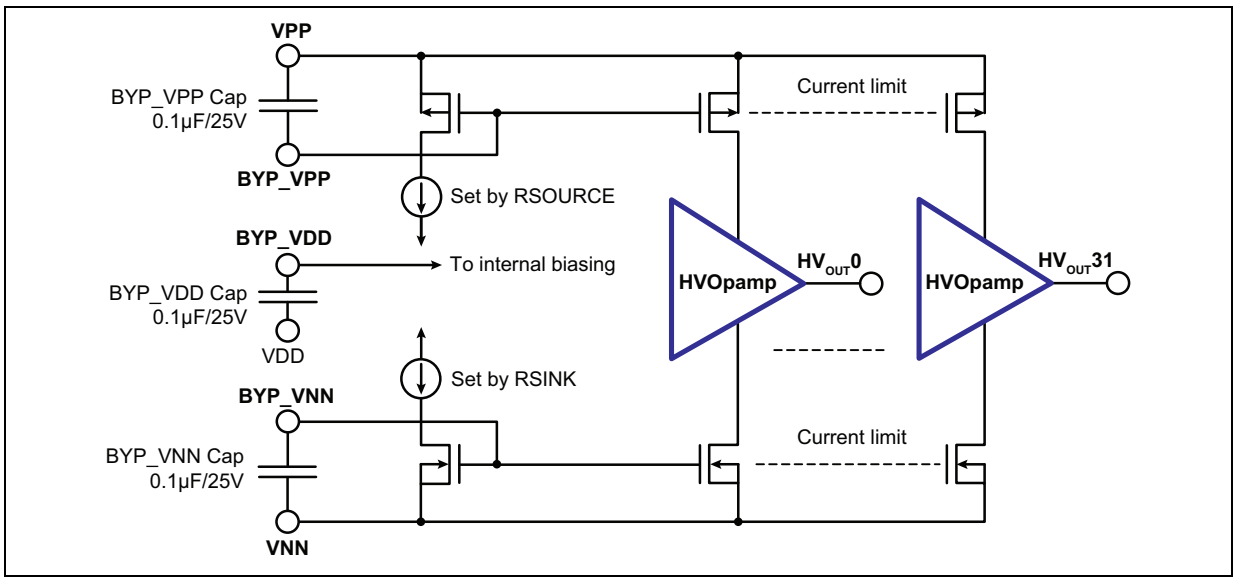


FIGURE 4-4: *Internal Reference Current Diagram.*

4.3 Ground Isolation (AGND/DGND Isolation)

It is important that the AGND pin is connected to a clean ground. The hold capacitors are internally connected to the AGND, and any ground noise will directly couple to the high-voltage outputs (with a gain of 72). The analog and digital ground traces on the PCB should be physically separated to reduce digital switching noise, degrading the signal to noise performance.

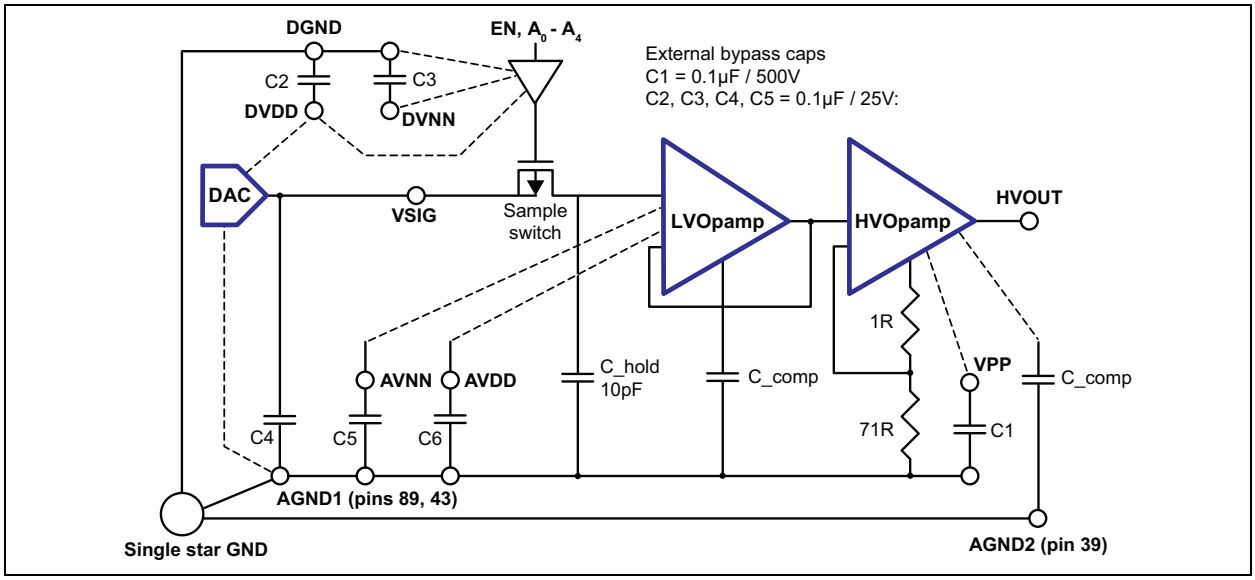
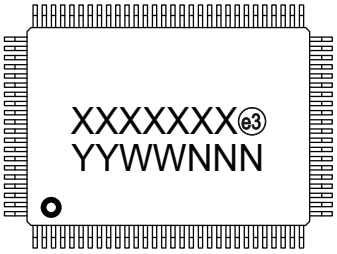


FIGURE 4-5: *AGND/DGND Ground Isolation.*

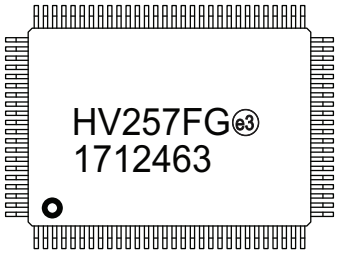
5.0 PACKAGE MARKING INFORMATION

5.1 Packaging Information

100-lead MQFP



Example

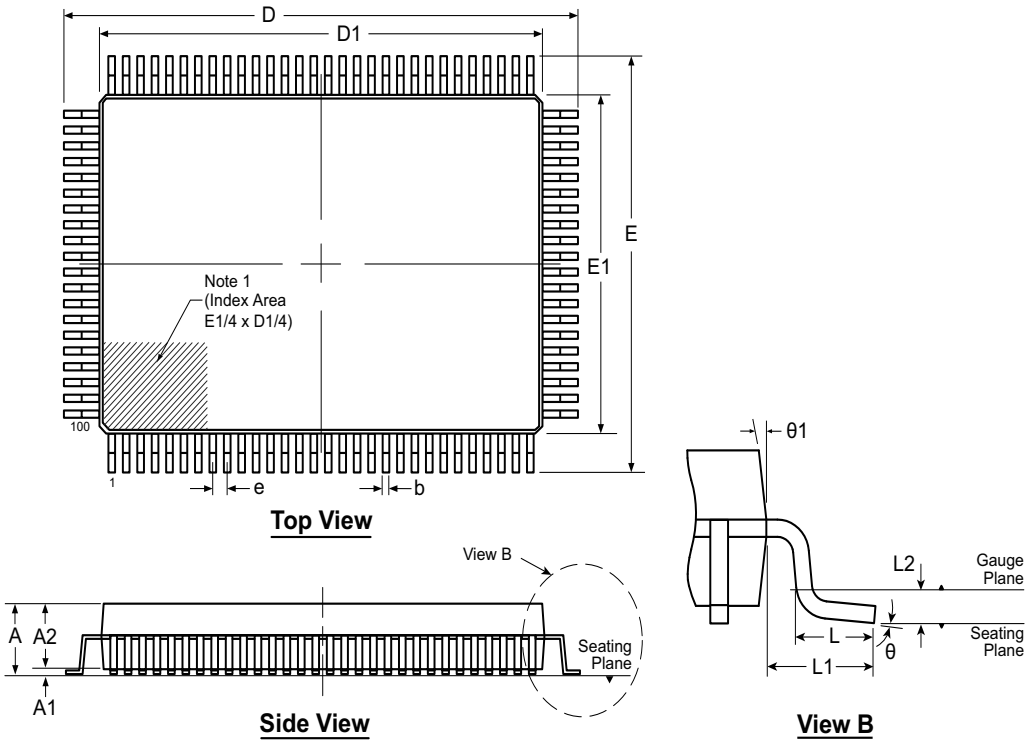


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

100-Lead MQFP Package Outline (FG)

20.00x14.00mm body, 3.15mm height (max), 0.65mm pitch, 3.20mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.50*	0.00	2.50	0.22	22.95*	19.80*	16.95*	13.80*	0.65 BSC	0.73	1.60 REF	0.25 BSC	0°	5°
	NOM	-	-	2.70	-	23.20	20.00	17.20	14.00		0.88			-	-
	MAX	3.15	0.25	2.90	0.40	23.45*	20.20*	17.45*	14.20*		1.03			7°	16°

JEDEC Registration MS-022, Variation GC-2, Issue B, Dec. 1996.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2017)

- Converted Supertex Doc# DSFP-HV257 to Microchip DS20005827A
- Changed the part marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV257	=	32-Channel High-Voltage Sample-and-Hold Amplifier Array
Package:	FG	=	100-lead MQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a K6 Package

Example:

a) HV257FG-G: 32-Channel High-Voltage Sample-and-Hold Amplifier Array, 100-lead MQFP, 66/Tray

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