SST25VF016B

16 Mbit SPI Serial Flash
EOL Supplemental Information

1.0 PRODUCT DESCRIPTION

The 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. The SST25VF016B devices are enhanced with improved operating frequency and even lower power consumption than the original SST25VFxxxA devices. SST25VF016B SPI serial flash memories are manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

This document provides supplemental information about the 75/80 MHz parts which are End-of-Life (EOL). Except for the information provided herein, the EOL parts behave as described in the SST25VF016B data sheet DS-20005044. See page 6 for specific part numbers.

2.0 DEVICE OPERATION

2.1 Instructions

Instructions are used to read, write (Erase and Program), and configure the SST25VF016B. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Byte-Program, Auto Address Increment (AAI) programming, Sector-Erase, Block-Erase, Write-Status-Register, or Chip-Erase instructions, the Write-Enable (WREN) instruction must be executed first. The complete list of instructions is provided in Table 2-1. All instructions are synchronized off a high to low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low to high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

TABLE 2-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory at 25 MHz	0000 0011b (03H)	3	0	1 to ∞	25 MHz
High-Speed Read	Read Memory at 80 MHz	0000 1011b (0BH)	3	1	1 to ∞	80 MHz
4 KByte Sector-Erase[3]	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0	80 MHz
32 KByte Block-Erase[4]	Erase 32 KByte block of memory array	0101 0010b (52H)	3	0	0	80 MHz
64 KByte Block-Erase[5]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0	80 MHz
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	80 MHz
Byte-Program	To Program One Data Byte	0000 0010b (02H)	3	0	1	80 MHz
AAI-Word-Program[6]	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞	80 MHz
RDSR[7]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	80 MHz
EWSR	Enable-Write-Status-Register	0101b 0000b (50H)	0	0	0	80 MHz
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1	80 MHz

TABLE 2-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
WREN	Write-Enable	0000 0110b (06H)	0	0	0	80 MHz
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	80 MHz
RDID[8]	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞	80 MHz
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞	80 MHz
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0	80 MHz
DBSY	Disable SO as RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0	80 MHz

0 25044

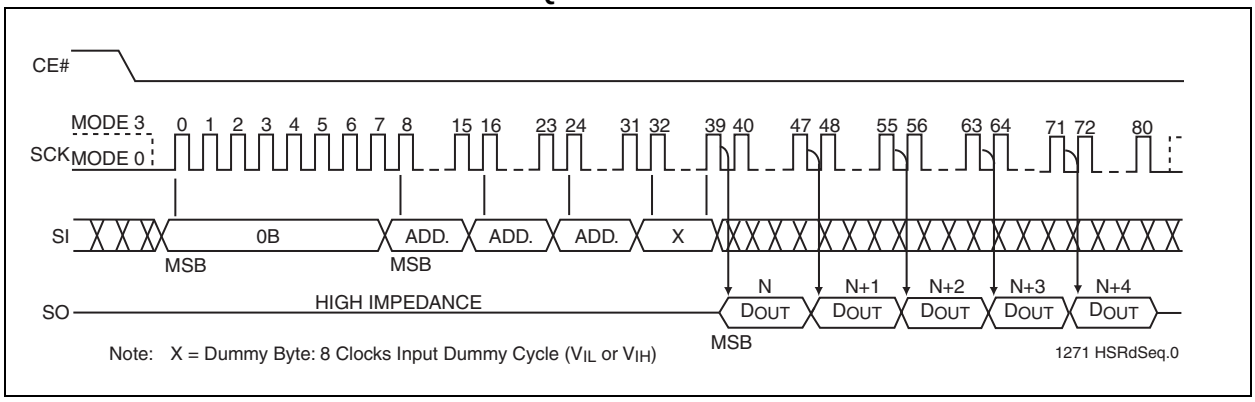
1. One bus cycle is eight clock periods.
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. 4KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
4. 32KByte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
5. 64KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A_{23}-A_1] with A_0=0, Data Byte 1 will be programmed into the initial address [A_{23}-A_1] with A_0=1.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
8. Manufacturer's ID is read with A_0=0, and Device ID is read with A_0=1. All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.

2.1.1 HIGH-SPEED-READ (80 MHZ)

The High-Speed-Read instruction supporting up to 80 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. CE# must remain active low for the duration of the High-Speed-Read cycle. See Figure 2-1 for the High-Speed-Read sequence.

Following a dummy cycle, the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 1FFFFFH has been read, the next output will be from address location 000000H.

FIGURE 2-1: HIGH-SPEED-READ SEQUENCE



3.0 ELECTRICAL SPECIFICATIONS

TABLE 3-1: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DDR}	Read Current		10	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@25 MHz, SO=open
I_{DDR2}	Read Current		15	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@50 MHz, SO=open
I_{DDR3}	Read Current		20	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@80 MHz, SO=open
I_{DDW}	Program and Erase Current		30	mA	CE#=V_{DD}
I_{SB}	Standby Current		20	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OL2}	Output Low Voltage		0.4	V	I_{OL}=1.6 mA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

TABLE 3-2: AC OPERATING CHARACTERISTICS

Symbol	Parameter	80 MHz		Units
		Min	Max	
F_{CLK}[1]	Serial Clock Frequency		80	MHz
T_{SCKH}	Serial Clock High Time	6		ns
T_{SCKL}	Serial Clock Low Time	6		ns
T_{SCKR}[2]	Serial Clock Rise Time (Slew Rate)	0.1		V/ns
T_{SCKF}	Serial Clock Fall Time (Slew Rate)	0.1		V/ns
T_{CES}[3]	CE# Active Setup Time	5		ns
T_{CEH}[3]	CE# Active Hold Time	5		ns
T_{CHS}[3]	CE# Not Active Setup Time	5		ns
T_{CHH}[3]	CE# Not Active Hold Time	5		ns
T_{CPH}	CE# High Time	50		ns
T_{CHZ}	CE# High to High-Z Output		7	ns
T_{CLZ}	SCK Low to Low-Z Output	0		ns
T_{DS}	Data In Setup Time	2		ns
T_{DH}	Data In Hold Time	4		ns
T_{HLS}	HOLD# Low Setup Time	5		ns
T_{HHS}	HOLD# High Setup Time	5		ns
T_{HLH}	HOLD# Low Hold Time	5		ns
T_{HHH}	HOLD# High Hold Time	5		ns
T_{HZ}	HOLD# Low to High-Z Output		7	ns
T_{LZ}	HOLD# High to Low-Z Output		7	ns
T_{OH}	Output Hold from SCK Change	0		ns
T_V	Output Valid from SCK		6	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms
T_{BP}	Byte-Program		10	µs

1. Maximum clock frequency for Read Instruction, 03H, is 25 MHz
2. Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements
3. Relative to SCK.

TABLE 3-3: REVISION HISTORY

Revision	Description	Date
A	• Initial release of EOL data sheet	Apr 2015

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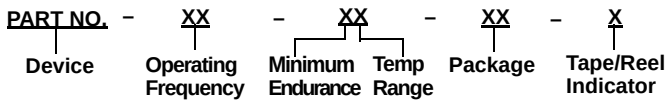

Device:	SST25VF016B	= 16 Mbit, 2.7-3.6V, SPI Flash Memory
Operating Frequency:	75	= 75 MHz (80 MHz)
Minimum Endurance	4	= 10,000 cycles
Temperature:	I	= -40°C to +85°C
	C	= 0°C to +70°C
Package:	QAE	= WSON (6mm x 5mm Body), 8-lead
	S2AE	= SOIC (200 mil Body), 8-lead
Tape and Reel Flag:	T	= Tape and Reel

Valid Combinations:

SST25VF016B-75-4I-S2AE
SST25VF016B-75-4I-S2AE-T
SST25VF016B-75-4I-QAE
SST25VF016B-75-4I-QAE-T

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