RE46C200

9V Programmable Photoelectric Smoke Detector ASIC

Features

- 6.5-12V Operation
- Low Quiescent Current
- Programmable Internal Infrared Emitter Diode (IRED) Current
- Programmable Standby Alarm Level
- Programmable Hush™ Alarm Level
- Programmable Hysteresis Alarm Level
- Programmable Chamber Test Alarm Level
- Programmable Low Battery Test
- Programmable Low-Battery Hush
- Programmable Horn Pattern
- Horn Synchronization
- 10-year End-of-Life Indication
- Differentiated Chamber Fail and Low Battery Warnings
- Local Alarm Memory
- Interconnect up to 40 Detectors
- IO Filter and Charge Dump
- Smart IO for CO alarm Option
- 9-Minute or 80-Second Hush Timer
- Smart Hush® Option
- Automatic Alarm Locate for Interconnected Units

Description

The RE46C200 is a next generation low power CMOS photoelectric-type smoke detector IC. With minimal external components, this circuit will provide all the required features for a photoelectric-type smoke detector.

The design incorporates a gain selectable photo amplifier for use with an infrared emitter/detector pair.

An on-chip oscillator strobes power to the smoke detection circuitry for 5 ms every 10 seconds to keep standby current to a minimum.

A check for a low battery condition is performed every 80 seconds and chamber test is performed once every 320 seconds when in standby. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

An interconnect pin allows multiple detectors to be connected such that when one unit alarms, all units will sound. A charge dump feature will quickly discharge the interconnect line when exiting a local alarm. The interconnect input is also digitally filtered.

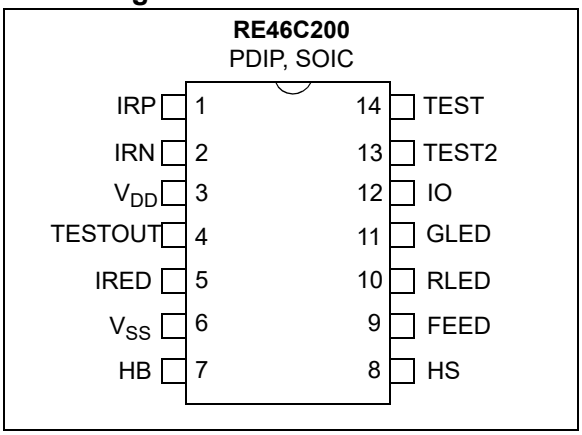
An internal 9-minute or 80-second timer is used for a Hush operation.

A local alarm memory feature allows the user to determine if the unit has previously entered a local alarm condition.

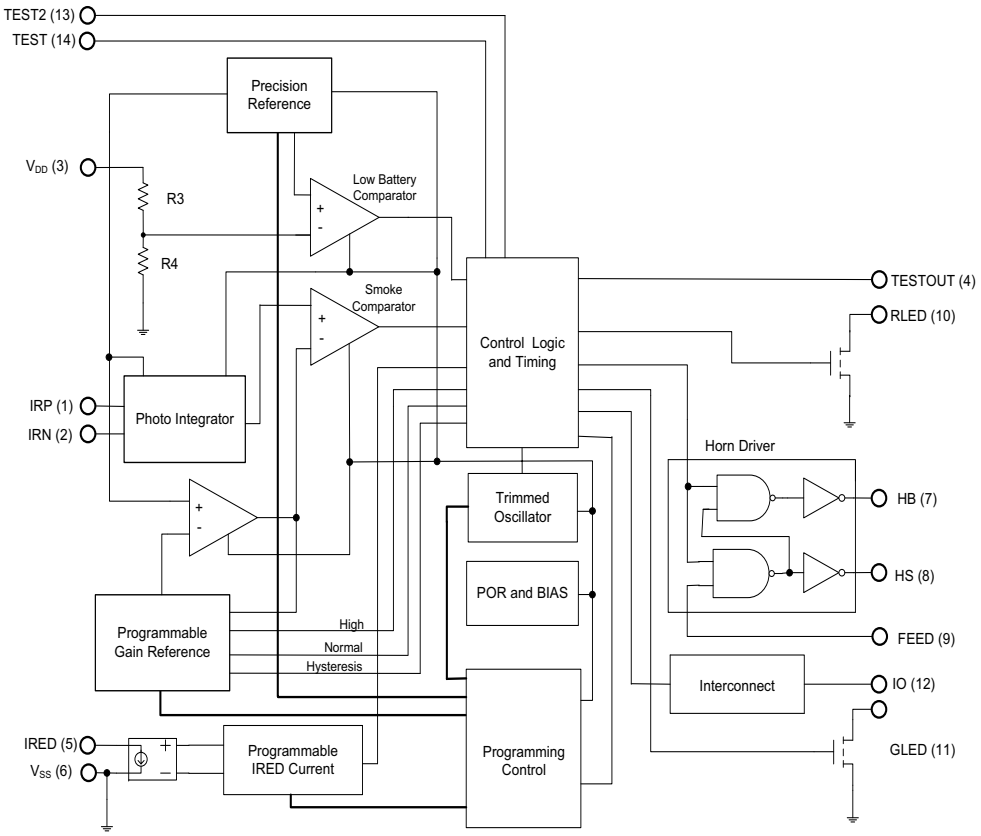
Utilizing low power CMOS technology, the RE46C200 is designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217 and UL268.

Pin Configuration

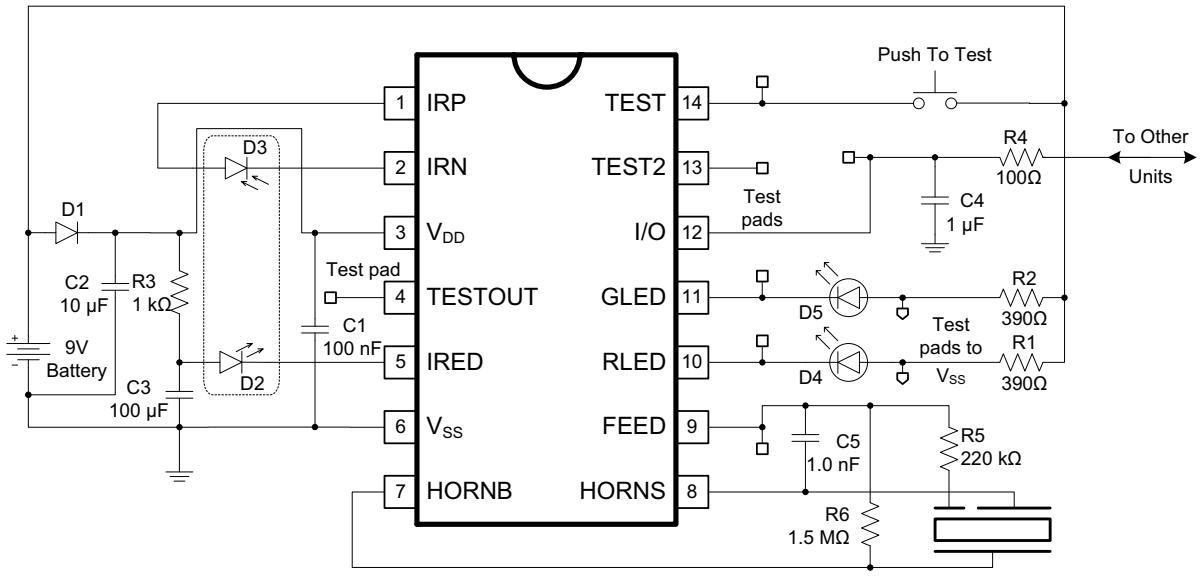
RE46C200
PDIP, SOIC



Functional Block Diagram



Typical Application



Note 1: R5, R6 and C5 are typical values and may be adjusted to maximize sound pressure.

2: C1 should be located as close as possible to the device power pins.

3: No internal reverse battery protection. External reverse battery protection (for example: D1) circuitry required.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{DD}.....12.5V
Voltage Range Except FEED, IO, IRP, IRN ..... .
.....V_{IN} = - .3 to V_{DD} + .3V
FEED Input Voltage Range..... V_{INFD} = -10 to + 22V
IO Input Voltage Range..... V_{IO1} = - .3 to 15V
IRP/IRN Input Voltage Range ..... V_{INIRD} = - .3 to 5.5V
Input Current Except FEED ..... I_{IN} = 10 mA
Operating Temperature ..... T_A = -10 to +60°C
Storage Temperature ..... T_{STG} = -55 to +125°C
Maximum Junction Temperature..... T_J = +150°C
MM ESD.....150V

†Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10 to +60°C, V_{DD} = 9V, V_{SS} = 0V (**Note 1**)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	3	6.5	—	12	V	Operating
Supply Current	I_{DD}	3	—	0.9	1.5	µA	Standby
Input Leakage	L_{INOP}	1	-200	—	200	pA	IRP = 5V or V_{SS}
		2	-200	—	200	pA	IRN = 5V or V_{SS}
	I_{HFD1}	9	—	20	50	µA	FEED = 22V
	I_{ILFD1}	9	-50	-15	—	µA	FEED = -10V
Input Voltage Low	V_{IL1}	9	—	—	2.7	V	FEED
	V_{IL2}	12	—	—	1	V	No local alarm, IO as an input
	V_{IL3}	13, 14	—	—	3.4	V	TEST or TEST2
Input Voltage High	V_{IH1}	9	6.2	—	—	V	FEED; V_{BST} = 9V
	V_{IH2}	12	3.0	—	—	V	No local alarm, IO as an input
	V_{IL3}	13, 14	5.6	—	—	V	TEST or TEST2
Input Pull Down Current	I_{PD1}	13,14	20	50	80	µA	V_{IN} = V_{DD}
Output Voltage High	V_{OH1}	7,8	5.5	—	—	V	I_{OH} = -16 mA, V_{DD} = 6.5V
Output Voltage Low	V_{OL1}	7,8	—	—	1	V	I_{OL} = 16 mA, V_{DD} = 6.5V
	V_{OL2}	10,11	—	—	0.6	V	I_{OL} = 10 mA, V_{DD} = 6.5V
Output Off Leakage High	I_{IOHZ}	10,11	—	—	1	µA	Outputs Off, V_{IN} = V_{DD}

Note 1: Production tested at room temperature with temperature guard-banded limits.

2: Not production tested.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10 to +60°C, V_{DD} = 9V, V_{SS} = 0V (**Note 1**)

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Output Current	I_{IOL1}	12	20	50	80	µA	$V_{IN} = V_{DD}$
	I_{IOL2}	12		—	150	µA	V_{IN} = 15v
	I_{IOH1}	12	-4	—	-16	mA	Alarm, V_{IO} = 4V or V_{IO}= 0V
	I_{IODMP}	12	5	—	—	mA	At Conclusion of Local Alarm or Test, V_{IO} = 1V
	I_{IRED50}	5	45	50	55	mA	IRED on; V_{IRED} = 1.5V; (50 mA option selected; T_A = +27°C)
	$I_{IRED100}$	5	90	100	110	mA	IRED on; V_{IRED} = 1.5V; (100 mA option selected; T_A = +27°C)
	$I_{IRED150}$	5	135	150	165	mA	IRED on; V_{IRED} = 1.5V; (150 mA option selected; T_A = +27°C
	$I_{IRED200}$	5	180	200	220	mA	IRED on; V_{IRED} = 1.5V; (200 mA option selected; T_A = +27°C)
IRED Temperature Coefficient	T_{CIRED}	5	—	0.5	—	%/ºC	IRED Output Current (**Note 2**)
Low Battery Alarm Voltage	V_{LB}	3	6.75	6.9	7.05	V	6.9V setting
			7.05	7.2	7.35	V	7.2V setting
			7.35	7.5	7.65	V	7.5V setting
			7.65	7.8	7.95	V	7.8V setting

Note 1: Production tested at room temperature with temperature guard-banded limits.

2: Not production tested.

AC ELECTRICAL CHARACTERISTICS

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 9V, V_{ss} = 0V.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Condition
Time Base							
Oscillator Period	T_{POSC}		593	625	657	µs	Operating, **Note 2**
Oscillator Pulse Width	T_{PW}		296	312	329	µs	Operating
Oscillator Tolerance	T_{TOL}		-5%	0	5%	%	Operating
Clock Period	T_{PCLK}		9.5	10	10.5	ms	Operating

Note 1: Typical values are for design information and not verified.

2: TPOSC is 100% production tested. All other timing is verified by functional testing.

3: See timing diagram for CO alarm horn pattern.

4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 9V, V_{ss} = 0V.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Condition
RLED Indicator							
LED On Time	T_{ON1}	10	9.5	10	10.5	ms	Operating
LED Off Time	T_{LOF1}	10	304	320	336	s	Standby, No Alarm
	T_{LOF2}	10	0.94	0.99	1.04	s	Local Alarm Condition
	T_{LOF3}	10	9.5	10	10.5	s	Timer mode, No Local Alarm
LED Period	T_{PLED0}	10	LED IS NOT ON				Remote Alarm only
	T_{PLED1}	10	304	320	336	s	Standby, No Alarm
	T_{PLED2}	10	0.95	1	1.05	s	Local Alarm Condition
	T_{PLED3}	10	9.5	10	10.5	s	Hush mode, No Local Alarm
GLED Indicator							
LED On Time	T_{ON1}	11	9.5	10	10.5	ms	Operating
LED Off Time	T_{OFLED1}	11	0.94	0.99	1.04	s	Alarm Memory LED Pulse Train (3x) Off Time
	T_{OFLED2}	11	36.1	38	39.9	s	Alarm Memory LED Off Time Between Pulse Train (3x)
	T_{LOF4}	11	228	240	252	ms	Alarm Memory Indication in PTT
LED Period	T_{PLED4}	11	238	250	263	ms	Alarm Memory Indication in PTT
	T_{PLED5}	11	38	40	42	s	Alarm Memory LED Timer Set
Alarm Memory Indication Timeout Period	T_{AMTO}	11	22.8	24	25.2	Hours	Alarm memory set, AMTO<2:1> = 00
			45.6	48	50.4	Hours	Alarm memory set, AMTO<2:1> = 01
			0	0	0	—	AMTO<2:1> = 10; No alarm memory indication
			∞	∞	∞	—	Alarm memory set, AMTO<2:1> = 11;
Smoke Check							
Smoke Test Period IRED	T_{STPER0}	4, 5	9.5	10	10.5	s	Standby, No Alarm
	T_{STPER1}	4, 5	0.95	1	1.05	s	Standby, one or more Valid Smoke Samples
	T_{STPER2}	4, 5	237	250	263	ms	Push button Test, not in alarm
	T_{STPER3}	4, 5	0.95	1	1.05	s	Local Alarm (three consecutive Valid Smoke Samples)
	T_{STPER4}	4, 5	9.5	10	10.5	s	In Remote Alarm
Chamber Test Period	T_{PCT1}	4, 5	304	320	336	s	Chamber Test, No Alarm

Note 1: Typical values are for design information and not verified.

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3: See timing diagram for CO alarm horn pattern.

4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 9V, V_{ss} = 0V.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Condition
IRED On Time	T_{IRON1}	5	—	110	—	µs	Operating/DIAG, **Note 1**
	T_{IRON2}	5	—	220	—	µs	Operating/DIAG, **Note 1**
	T_{IRON3}	5	—	330	—	µs	Operating/DIAG, **Note 1**
	T_{IRON4}	5	—	440	—	µs	Operating/DIAG, **Note 1**
Low Battery							
Low Battery Check Period	T_{PLB1}		76	80	84	s	Standby, no alarm, RLED off
	T_{PLB2}		304	320	336	s	Standby, no alarm, RLED on
Horn Operation							
Horn Startup Delay	T_{HDLY1}	7,8	475	500	525	ms	From local alarm to horn active, temporal horn pattern
	T_{HDLY2}	7,8	380	400	420	ms	From local alarm to horn active, continuous horn pattern
Horn Period	T_{HPER1}	7,8	38	40	42	s	Low Battery, No Alarm
	T_{HPER2}	7,8	38	40	42	s	Chamber Fail, No Alarm
	T_{HPER3}	7,8	237	250	263	ms	Alarm Memory Active, Push-to-Test
	T_{HPER4}	7,8	5.5	5.8	6.1	s	CO alarm horn period, **Note 3**
	T_{HPER5}	7,8	0.47	0.5	0.53	s	Operating, Alarm Condition, **Note 4**; Continuous horn pattern
	T_{HPER6}	7,8	3.8	4	4.2	s	Operating, Alarm Condition, **Note 4**; Temporal horn pattern
Horn On Time	T_{HON1}	7,8	9.5	10	10.5	ms	Low Battery or Fail Chamber test, No Alarm, or optional PTT in Alarm Memory
	T_{HON2}	7,8	475	500	525	ms	Operating, Alarm Condition, **Note 4**; Temporal horn pattern
	T_{HON3}	7,8	332	350	368	ms	Operating, Alarm Condition, **Note 4**; Continuous horn pattern
	T_{HON4}	7,8	95	100	105	ms	CO alarm, **Note 3**

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5: See timing diagram for horn synchronization and AAL.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 9V, V_{ss} = 0V.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Condition
Horn Off Time	T_{HOF1}	7,8	475	500	525	ms	Operating, Alarm Condition, **Note 4**; Temporal horn pattern
	T_{HOF2}	7,8	1.43	1.5	1.58	s	Operating, Alarm Condition, **Note 4**; Temporal horn pattern
	T_{HOF3}	7,8	143	150	158	ms	Operating, Alarm Condition, **Note 4**; Continuous horn pattern
	T_{HOF4}	7,8	37	39	41	s	Chamber Fail Horn Off Time
	T_{HOF5}	7,8	466	490	515	ms	Chamber Fail Horn Pulse Train Off Time
	T_{HOF6}	7,8	95	100	105	ms	CO alarm horn off time between pulses, **Note 3**
	T_{HOF7}	7,8	4.8	5.1	5.4	s	CO alarm horn off time between pulse trains, **Note 3**
	T_{HOF8}	7,8	38	40	42	s	Low Battery, No Alarm
	T_{HOF9}	7,8	228	240	252	ms	Alarm Memory Indication in PTT
Hush Timer Operation							
Hush Timer Period	T_{TPER}		8.5	9	9.5	Min	**9 minute option** No Alarm Condition
			76	80	84	s	>1 minute option No Alarm Condition
EOL (End-of-Life)							
End-of-Life Sample Period	T_{EOLPER}		346	364	382	Hours	Standby, no alarms
End-of-Life (timeout)	T_{EOLTO}		9.5	10	10.5	Years	Standby, no alarms, time to EOL warning
Interconnect							
IO Active Delay	T_{IODLY1}	12	3.5	3.7	3.9	s	Local Alarm Start to IO Active
Remote Alarm Delay	T_{IODLY2}	12	0.77	0.81	0.86	s	Temporal Horn Pattern, No Local Alarm, IO Active to Alarm
	T_{IODLY3}	12	0.29	0.31	0.34	s	Continuous Horn Pattern, No Local Alarm, IO Active to Alarm
IO Filter	T_{IOFILT}	12			290	ms	IO pulse width filtered
IO Pulse On Time for CO Alarm	T_{IOPW1}	12	23	—	290	ms	No local alarm, two valid pulses required for CO
IO Pulse Off Time for CO Alarm	T_{IOTO1}	12	—	—	5.4	s	IO = Low
IO Charge Dump Duration	T_{IODMP}	12	475	500	525	ms	At Conclusion of Local Alarm or Test

Note 1: Typical values are for design information and not verified.

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3: See timing diagram for CO alarm horn pattern.

4: See timing diagram for temporal and continuous horn pattern.

5: See timing diagram for horn synchronization and AAL.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -10° to +60°C, V_{DD} = 9V, V_{ss} = 0V.

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Condition
Horn Synchronization							
IO Pulse Period	T_{PIO1}	12	3.8	4	4.2	s	Local alarm, temporal horn pattern, SyncEn = 1, **Note 5**
IO Pulse On Time	T_{ONIO}	12	3.41	3.59	3.77	s	Local alarm, temporal horn pattern, SyncEn = 1, **Note 5**
Horn Sync IO Dump	T_{IODMP2}	12	95	100	105	ms	Local alarm, SyncEn = 1, IO dump active, **Note 4**
Horn Sync IO Dump Delay	T_{IODLY4}	12	285	300	315	ms	Local alarm, SyncEn = 1, **Note 5**
Horn Sync Contention Window	T_{IOCW}	12	294	310	326	ms	Local alarm, SyncEn = 1, IO = 0, no IO dump, IO pull-down, **Note 5**
Auto Alarm Locate (AAL)							
IO Cycle Period	T_{PIO2}	12	15.2	16	16.8	s	Local alarm, temporal horn pattern, SyncEn = 1, NoAAL = 0, **Note 5**
IO Cycle Off Time	T_{OFIO}	12	4.19	4.41	4.63	s	Local alarm, temporal horn pattern, SyncEn = 1, NoAAL = 0, IO off time between IO pulse trains (3x), **Note 5**
Test Mode							
Input Pulse Width in Test modes	T_{TMPW}	9,12,	10			µs	Input Pulse width, high or low
		13,14					Inputs FEED, IO, TEST2, TEST
Data Setup Time In Serial Read/Write modes	T_{TMSU}	9,14	10			µs	Data(TEST) setup time before CLK(FEED) in TM1/3/19
Data Hold Time In Serial Read/Write modes	T_{TMH}	9,14	10			µs	Data(TEST) hold time before CLK(FEED) in TM1/3/19
Clock Period In Serial Read/Write modes	T_{TMP}	9	30			µs	CLK(FEED) in TM1/3, with minimum pulse width, setup, and hold times
Programming Pulse Width	T_{PROG}	12	10		20	ms	IO high in TM1/3/11/15/19
Detection Enable Pulse Width	$T_{DETP}W$	9	2			ms	Detection Enable (FEED) high for full detection in TM4-7/10/12-15
Detection Enable Setup	T_{DETSU}	9	2			ms	Detection Enable (FEED) low before enabling detection measurement in TM4-7/10/12-15

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5: See timing diagram for horn synchronization and AAL.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-10	—	+60	°C	
Storage Temperature Range	T_{STG}	-55	—	+125	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-SOIC (150 mil.)	θ_{JA}	—	90.8	—	°C/W	
Thermal Resistance, 14L-PDIP (300 mil.)	θ_{JA}	—	70	—	°C/W	

NOTES:

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

RE46C200 PDIP, SOIC	**Symbol**	**Function**
1	IRP	This is the anode input for the smoke chamber photo diode.
2	IRN	This is the cathode input for the smoke chamber photo diode.
3	V_{DD}	Connect to the positive supply voltage
4	TESTOUT	This output is an indicator of the internal IO dump signal and smoke test signal. This pin is also used for test modes.
5	IRED	This current driver sinks a controlled pulsed current from the Infrared Emitting Diode during a smoke test sample.
6	V_{SS}	Connect to the negative supply voltage
7	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
8	HS	This pin is a complementary output to HB, connected to the ceramic electrode of the piezoelectric transducer.
9	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to V_{DD} or V_{SS}.
10	RLED	Open drain NMOS output, used to drive a visible LED. This pin provides the load current for the low battery test, and is a visual indicator for alarm and Hush mode.
11	GLED	Open drain NMOS output, used to drive a visible LED to provide visual indication of an alarm memory condition.
12	IO	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull down device and a charge dump device.
13	TEST2	Test input to invoke test modes. This pin has an internal pull down.
14	TEST	This input is used to invoke push-to-test, Timer mode, and alarm memory indication. This input has an internal pull down.

NOTES:

3.0 DEVICE DESCRIPTION

3.1 Standby Internal Timing

The internal oscillator is trimmed to ±5% tolerance. The oscillator period is 625 µs. A clock divider generates the 10 ms system clock.

In Standby, once every 10 seconds, the smoke detection circuitry is powered on for 5 ms. At the conclusion of the 5 ms, a smoke check measurement is made and the status of the smoke comparator is latched. If a smoke condition is present, the period to the next smoke check measurement decreases and additional checks are made.

In Standby, once every 80 seconds, the low battery detection circuitry is powered on for 10 ms. At the conclusion of the 10 ms, the status of the low battery comparator is latched. RLED is enabled for 10 ms every 320 seconds to provide a current load in the loaded battery test.

In Standby, once every 320 seconds, the chamber test circuitry is powered on for 5 ms. At the conclusion of the 5 ms, the status of the chamber test is latched (see **Section 3.4 "Chamber Test"** for details).

3.2 Smoke Detection Circuitry

The smoke detection circuitry consists of a integrating photo amplifier with gain and an ADC. The ADC is composed of a DAC, comparator and counter circuitry. The counter circuitry increments the DAC output voltage until the DAC output voltage is equal to or greater than the photo amp output voltage.

A smoke check involves two steps. First, a dark integration measurement is made and digitized with the IRED off. Then a lit integration is made and digitized with the IRED on. The difference of the digitized values of the two integrations is compared to the alarm limit to determine if a smoke detection occurred. The dark integration is made to null out any offsets or leakage effects.

Three consecutive smoke detections will cause the device to go into local alarm and the horn circuit and interconnect will be active. If one or more valid smoke samples are detected, the RLED will turn on for 10 ms at a 1 Hz rate. When a local alarm occurs, the hysteresis alarm limit is selected to provide alarm hysteresis. The hysteresis limit must be less than the local alarm limit. All alarm limits are user-programmable.

The integrating photo amp gain and integration time are user-programmable. The combination of programmable gain and integration time allows an acceptable signal level to be achieved in different ways. The programmable integration time also sets the IRED on time. The IRED current drive is all internal and user-programmable as well.

The integrating photo amp has three separate gain modes for a selected gain:

- Normal Gain for Standby and Local Alarm
- Low Gain for Hush Timer
- High Gain for Chamber Test and Push-to-Test

There are four separate sets of alarm limits (all user-programmable):

- Local Alarm Limit
- Hysteresis Alarm Limit
- Hush Alarm Limit
- Chamber Test Alarm Limit

The combination of programmable gain, integration time, IRED current, and alarm limits provides a high degree of flexibility when designing a smoke detector.

3.3 Photo Chamber Long Term Drift (LTD) Adjust

Photo chamber long term drift adjustment (LTD) is a user-programmable option.

If this option is selected, during calibration a normal no-smoke baseline integration measurement is made and stored in EEPROM. Then, during normal operation, a new baseline is calculated by making 64 integration measurements over a period of 8 hours. These measurements are averaged and compared to the original baseline stored during calibration to calculate the long term drift. Only the Normal, Hysteresis and Hush alarm limits are adjusted by the LTD calculation. The Chamber Test alarm limit is not adjusted by the LTD calculation. Drift sampling is suspended during Hush, local smoke and remote smoke conditions.

The long term drift also has a maximum limit, LTD_{max}. This programmed value limits long term drift to a maximum value, so that the positive drift adjustment has a ceiling. There is no minimum programmable long term drift limit. The LTD_{max} limit is used to keep the drift adjustment within reasonable bounds. When the LTD_{max} limit is reached, a chamber fail warning is sounded (see **Section 3.4 "Chamber Test"**).

The LTD_{max} value must be greater than the stored LTD value. An LTD_{max} value less than the LTD value can cause an error in the LTD calculation. If LTD_{max} is not used, then it should be programmed to 63.

3.4 Chamber Test

Once every 320 seconds a smoke test with high gain settings is performed to test the photo-chamber function. This check of the chamber is made by amplifying background reflections to simulate a smoke condition.

If two consecutive chamber tests fail to detect a simulated smoke condition, then the chamber fail latch is set and the failure warning is generated. The horn will chirp three times every 40s. Each chirp is 10 ms long and three chirps are spaced at a 0.5s interval. The chamber fail warning chirp is separated from the low-battery warning chirp by about 20s (see **Section 3.5 "Low Battery Detection"**).

The horn will continue this pattern until the chamber fail latch is reset. The reset occurs when any one of the followings is active:

- Two consecutive chamber tests pass
- Local smoke alarm
- PTT smoke alarm

Chamber test is performed approximately 140s after loaded low battery test.

In local alarm, PTT alarm, or remote alarm condition, the chamber test is not performed, and the low battery chirping is prohibited.

3.5 Low Battery Detection

Once every 80 seconds, the status of the battery voltage is checked by comparing a fraction of V_{DD} voltage to an internal reference voltage. In each period of 320 seconds, the battery voltage is checked four times. Of these four battery checks, three are unloaded and one is loaded with the RLED turned on which provides a current load on the battery. Low battery status is latched at the end of the 10 ms RLED pulse.

If the low battery test fails, the horn will chirp for 10 ms every 40 seconds, and will continue to chirp until the next low battery check is passed. The unloaded low battery checks are skipped in low battery condition.

As a user-programmable option, a Low-Battery Hush mode can be selected. If a low battery condition exists, upon release of PTT, the unit will enter Low-battery Hush mode and the 10ms horn chirp will be silenced for 8 hours. At the conclusion of the 8 hours, the audible indication will resume if the low battery condition still exists.

3.6 Push-To-Test Operation (PTT)

PTT occurs when TEST is driven high (V_{IH3}). Release of PTT occurs when TEST is driven low (V_{IL3}).

PTT has different functions for different circumstances.

In Standby, PTT tests the unit. Upon start of PTT, the photo amplifier High Gain mode is selected and background reflections are used to emulate a smoke condition. The smoke detection rate increases to once every 250 ms. After three consecutive smoke detections, the unit will go into a Local Alarm condition. In alarm, the smoke detection rate decreases to once every 1s. Upon release of PTT, the photo amplifier normal gain is selected, with hysteresis alarm levels. The detection rate remains at once every second until three consecutive no-smoke conditions are detected.

In Standby and if the alarm memory latch is already set, PTT does not test the unit. PTT invokes the alarm memory indication. Depending on the user selection, it can be a 4 Hz horn chirp, 4 Hz GLED pulse, or both. Upon release of PTT, the alarm memory latch is reset.

In Standby and in low battery condition, PTT tests the unit and RLED will be constantly enabled. This allows the user to easily identify the low battery unit without waiting for 40s to hear a horn chirp. Upon release of PTT, RLED goes back to normal standby pulse rate. The Low-Battery Hush mode is then activated, if this function is enabled.

3.7 Interconnect Operation

The bidirectional IO pin allows multiple detectors to be interconnected. In a Local Alarm condition, this pin is driven high 3.7s after a Local Alarm condition is sensed through a constant current source; this amounts to 4s of originating alarm before remote alarms sound. Shorting this output to ground will not cause excessive current to flow. The IO is ignored as an input during a Local Alarm.

The IO pin also has an NMOS discharge device that is active for 0.5s after the conclusion of any type of local alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 310 ms nominal digital filter. This allows for interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

As a user-programmable option, the smart interconnect (smart IO) function can be selected. If the IO input is pulsed high twice with a nominal pulse on time greater than 23 ms and within 5.4s, a CO alarm condition is detected and the CO temporal horn pattern will sound. The CO temporal horn pattern will sound at least two times if a CO alarm condition is detected.

3.8 Hush Timer Mode

In Hush mode, the photo amp gain is reduced by one half and the Hush alarm level, which is user-programmable, sets the smoke detection level. RLED is turned on for 10 ms every 10s while in Hush mode.

The Hush mode period is user-programmable and can be set to either 9 minutes or 80s. After this period times out, the unit goes back to standby operation.

Upon release of PTT, the unit may or may not go into a Hush mode, depending on the user selection.

If the Hush-In-Alarm-Only option is selected, then release of PTT only in a Local Alarm condition can initiate a Hush mode. Upon release of PTT, the unit is immediately reset out of alarm and the horn is silenced.

If the Hush-In-Alarm-Only option is not selected, then anytime a release of PTT occurs the Hush mode is initiated.

If the unit is currently in a Hush mode, then PTT will test the unit with the standby gain and alarm level. Upon release of PTT, a new Hush mode will be initiated.

As another user-programmable option, Hush mode can be terminated early by a Smart Hush function. This function allows the Hush mode to be canceled by either a high local smoke alarm or a remote smoke alarm. High local smoke alarm is a local smoke alarm caused by a smoke level which exceeds the Hush alarm level.

3.9 Local Alarm Memory

The Local Alarm Memory is a user-programmable option.

If a unit has entered a Local Alarm, then, when it exits the Local Alarm, the Alarm Memory latch is set. The GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED is pulsed on three times every 40s. Each GLED pulse is 10 ms long and spaced 1s from the next pulse. This local alarm memory indication can be disabled or displayed with a period of 24 hours, 48 hours, or no limit, depending on the user selection. This visual GLED indication is not displayed if a low battery condition exits.

The user will be able to identify a unit with an active local alarm memory anytime by PTT. Upon start of PTT, the local alarm memory indication will be activated. Depending on the user selection, it can be 4 Hz horn chirp, 4 Hz GLED pulse, or both. A release of PTT will reset the local alarm memory latch.

3.10 End-of-Life (EOL) Indicator

The EOL indicator is a user-programmable function.

If the EOL indicator function is enabled, then approximately every 15 days of continuous standby operation, the design will read an age count stored in EEPROM and will then increment this age. After 10 years of operation, an audible indication will be given to signal that the unit should be replaced. The EOL indicator is the same as the chamber test failure warning.

3.11 Horn Pattern

The smoke alarm horn pattern can be either a temporal horn pattern or a continuous horn pattern, depending on user selection. The temporal horn pattern supports the NFPA 72 emergency evacuation signal. The continuous horn pattern is a 70% duty cycle 2 Hz continuous horn pattern.

If a CO alarm is detected through the IO, the unit will sound the CO horn pattern. The CO horn pattern consists of 4 horn beeps in every 5.8s. Each horn beep is 100 ms long and separated by 100 ms.

3.12 Horn Synchronization

The horn synchronization function is a user-programmable function.

In an interconnected system, if one unit goes into local alarm, then other units will go into remote alarm. The IO line is driven high by the origination local smoke unit and stays high during the alarm.

If the horn synchronization function is enabled, then at the end of every temporal horn pattern and when horn is off, the origination unit will drive IO low, then high again. This periodic IO pulsing high and low will cause the remote smoke units to go into and out of remote alarm repeatedly. Each time when a unit goes into remote alarm, its timing is reset. The horn sound of all remote smoke units will be synchronized with the horn sound of the origination unit.

A protection circuit ensures that the unit that goes into local alarm first will be the master unit which conducts the horn synchronization. The units which go into local alarm later will not drive the IO line. This avoids bus contention problems.

This function works with the temporal horn pattern only.

3.13 Auto Alarm Locate

Auto Alarm Locate (AAL) is also a user-programmable function. AAL may be used with either temporal or continuous horn patterns. To use AAL with the temporal horn pattern, the horn synchronization function has to be selected also.

The purpose of AAL is to let users quickly find the local alarm units just by listening. The local alarm units will sound the horn pattern without interruption. The remote alarm units will sound the pattern with interruption. Every 16s the remote units are silenced for 4.7s.

The originating unit conducts the IO cycling. During every fourth temporal horn pattern, the IO is driven low for one temporal horn pattern. In the remaining three temporal horn patterns, the IO is still pulsing to keep the horn synchronized. For continuous horn patterns, the IO sends no synchronization pulse, but drives IO low for 4.4s to cause a 4.7s silence on remote alarms.

The RLED of the origination unit and other local smoke units will be turned on 10 ms every 1s. The RLED of the remote smoke units will be off.

4.0 USER PROGRAMMING MODES

The RE46C200 provides user programming and test modes. User programming modes allow the various device options to be set and stored in EEPROM. Test modes provide a means to evaluate device performance.

Table 4-1 lists the various parametric settings provided by the RE46C200. The IRED period also sets the photo amp integration time. The photo detection limits section shows the typical maximum input current range for a given gain factor and integration time of the photo amp. The photo detection resolution section shows the step resolution for a given gain factor and integration time of the photo amp. Table 4-2 provides a list of user-selectable features such as Hush and Alarm Memory options.

TABLE 4-1: PARAMETRIC PROGRAMMING

Parametric Programming		Range		Resolution
IRED Period		100 – 400 µs		100 µs
IRED Current		50 – 200 mA		50 mA
Low Battery Detection Voltage		6.9 – 7.8V		300 mV
Photo Detection Limits		**Input Current Range (nanoamps)**		
		Normal/Hysteresis	**Hush**	**Chamber Test**
Integration Time 100 µs	GF = 1x	61	122	30.5
	GF = 2x	30.5	61	15.3
	GF = 4x	15.3	30.5	7.6
	GF = 8x	7.6	15.3	3.8
Integration Time 200 µs	GF = 1x	30.5	61	15.3
	GF = 2x	15.3	30.5	7.6
	GF = 4x	7.6	15.3	3.8
	GF = 8x	3.8	7.6	1.91
Integration Time 300 µs	GF = 1x	20.3	40.7	10.2
	GF = 2x	10.2	20.3	5.1
	GF = 4x	5.1	10.2	2.54
	GF = 8x	2.54	5.1	1.27
Integration Time 400 µs	GF = 1x	15.3	30.5	7.6
	GF = 2x	7.6	15.3	3.8
	GF = 4x	3.8	7.6	1.91
	GF = 8x	1.91	3.8	0.95
Photo Detection Resolution		**Step Resolution (picoamps)**		
		Normal/Hysteresis	**Hush**	**Chamber Test**
Integration Time 100 µs	GF = 1x	1000	2000	500
	GF = 2x	500	1000	250
	GF = 4x	250	500	125
	GF = 8x	125	250	63
Integration Time 200 µs	GF = 1x	500	1000	250
	GF = 2x	250	500	125
	GF = 4x	125	250	63
	GF = 8x	63	125	31
Integration Time 300 µs	GF = 1x	333	667	167
	GF = 2x	167	333	83
	GF = 4x	83	167	42
	GF = 8x	42	83	21
Integration Time 400 µs	GF = 1x	250	500	125
	GF = 2x	125	250	63
	GF = 4x	63	125	31
	GF = 8x	31	63	16

TABLE 4-2: FEATURES PROGRAMMING

Features	Options
User Program Lockbit: Disables Programmability	Locked/Unlocked
Photo Chamber Long Term Drift Adjustment	Enable/Disable
Low Battery Detection Selection	6.9V, 7.2V, 7.5V, 7.8V
10 Year End-of-Life Indicator	Enable/Disable
Smart IO with CO Alarm Sensing	Enable/Disable
Auto Alarm Locate	Enable/Disable
Horn Synchronization	Enable/Disable
Low-Battery Hush	Enable/Disable
Alarm Memory Indicator at PTT: Horn Chirping	Enable/Disable
Alarm Memory Indicator at PTT: GLED Flashing	Enable/Disable
Alarm Memory Indicator at Standby Time Out Period	0/24/48 hour or no limit
Alarm Memory	Enable/Disable
Hush Time Out Period	9 minutes or 80 seconds
Smart Hush	Enable/Disable
Hush In Alarm Only	Enable/Disable
Hush	Enable/Disable
Horn Pattern Select	Temporal or Continuous

4.1 Calibration and Programming Procedures

Fifteen separate programming and test modes are available for user customization. The TEST2 input is used to enter these modes and step through these modes. To enter these modes, after power-up, TEST2 must be driven to V_{DD} and held at that level. To step through the modes, first the TEST input must be driven to V_{DD}. TEST2 is then clocked. TEST has to be high when clocking TEST2.

Anytime TEST2 and TEST are both driven to low, the unit will come out of these modes and go back to the Normal Operation mode. FEED, IO, and TEST are reconfigured to become test mode inputs. TEST2 clock occurs on the rising edge, when it switches from V_{SS} to V_{DD}. The test mode functions are outlined in the Table 4-3.

TABLE 4-3: TEST MODE FUNCTIONS

Mode	Description	TEST2 Clock	TEST	TEST2	FEED	IO	TESTOUT	RLED	GLED	HB
M0 (1)	Normal Operation	0	PTT/Hush	0	FEED	IO	IO Dump or Smoke check (2)	RLED	GLED	HB
TM0 (1)	Horn Test	1	HornEn	V_{DD}	FEED	IO	NA	RLED	GLED	HB
TM1	Serial Read/Write	2	ProgData	V_{DD}	ProgClk	ProgEn	Serial Out	RLED	GLED	HB
TM2	Low Battery Test	3	TEST	V_{DD}	FEED	VDD	LBCompOut (3)	RLED	GLED	HB
TM3	EOL Serial Read/Write	4	ProgData	V_{DD}	ProgClk	ProgEn	Serial Out	RLED	GLED	HB
Smoke Check Test Modes										
TM4	Chamber Test Limit Check (7)	5	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM5	Standby Limit Check (8)	6	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM6	Hysteresis Limit Check (9)	7	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)
TM7	Hush Limit Check	8	V_{DD}	V_{DD}	Measure Enable	V_{SS}	DCMP (4)	DAC (5)	IntegOut (6)	SCMP (4)

Note 1: After power-up, the unit is in M0, the Normal Operation mode. In M0, if TEST2 is driven to V_{DD}, the unit will enter TM0.

2: In M0, the digital output TESTOUT is driven to V_{DD} when the internal IO dump signal or the smoke check signal or the POR signal occur.

3: LBCompOut – digital comparator output (high if V_{DD} < LB trip point; low if V_{DD} > LB trip point).

4: The Digital Compare (DCMP) asserts as high when the digitized smoke level equals or exceeds the smoke alarm limit and SCMP is the latched DCMP value.

5: DAC – smoke level digitizer output voltage.

6: IntegOut – Integrator voltage level, including gain factor amplification.

7: Chamber Test Limit and PTT Limit Check should be set so that the test always produces a smoke condition (=1) in clear air.

8: Standby Smoke Check should be set so that it always tests positive (= 1) for minimum required smoke for alarm.

9: Hysteresis Smoke Check should be set so that it always produce a No Smoke (= 0) for maximum allowable smoke.

10: In LTD Cal mode, a smoke measurement increments the LTD counter.

11: In LTD Cal mode, the LTD shift register is set to the LTD counter when TEST = 0 for programming in TM11.

12: In LTD Cal mode, the LTD_{max} shift register is set to the LTD counter when TEST = 1 for programming in TM11.

13: ScmpOut asserts a high when the DAC output voltage is equal to or greater than the Integrator output voltage.

14: In calibration modes, TEST resets the dark integration measurement, after which the first Calibration Clock (CalCLK) on FEED causes a dark integration measurement.

15: CalCLK causes an integration with IRED on, starting with the rising edge; it also increments the DAC input by 1 on the falling edge.

TABLE 4-3: TEST MODE FUNCTIONS (CONTINUED)

Mode	Description	TEST2 Clock	TEST	TEST2	FEED	IO	TESTOUT	RLED	GLED	HB
Long Term Drift (LTD) Calibration Test Modes										
TM10	LTD Baseline	11	0	V_{DD}	Measure Enable (10)	Latch (11)	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
	Increment LTD Counter		⤴⤵		V_{SS}	V_{SS}				
	LTDmax		1		V_{SS}	Latch (12)				
TM11	Program LTD Values	12	Not Used	V_{DD}	V_{SS}	ProgEn	NA	NA	NA	HB
Smoke Calibration Test Modes										
TM12	Chamber Test Calibration	13	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM13	Standby Calibration	14	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM14	Hysteresis Calibration	15	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM15	Hush Calibration	16	Measure Enable (14)	V_{DD}	CalCLK (15)	Latch ProgEn	ScmpOut (13)	DAC (5)	IntegOut (6)	HB
TM19	EE Lock Bit	20	V_{DD}	V_{DD}	FEED	ProgEn	Lock Out	RLED	GLED	HB

Note 1: After power-up, the unit is in M0, the Normal Operation mode. In M0, if TEST2 is driven to V_{DD}, the unit will enter TM0.

2: In M0, the digital output TESTOUT is driven to V_{DD} when the internal IO dump signal or the smoke check signal or the POR signal occur.

3: LBCompOut – digital comparator output (high if V_{DD} < LB trip point; low if V_{DD} > LB trip point).

4: The Digital Compare (DCMP) asserts as high when the digitized smoke level equals or exceeds the smoke alarm limit and SCMP is the latched DCMP value.

5: DAC – smoke level digitizer output voltage.

6: IntegOut – Integrator voltage level, including gain factor amplification.

7: Chamber Test Limit and PTT Limit Check should be set so that the test always produces a smoke condition (=1) in clear air.

8: Standby Smoke Check should be set so that it always tests positive (= 1) for minimum required smoke for alarm.

9: Hysteresis Smoke Check should be set so that it always produce a No Smoke (= 0) for maximum allowable smoke.

10: In LTD Cal mode, a smoke measurement increments the LTD counter.

11: In LTD Cal mode, the LTD shift register is set to the LTD counter when TEST = 0 for programming in TM11.

12: In LTD Cal mode, the LTD_{max} shift register is set to the LTD counter when TEST = 1 for programming in TM11.

13: ScmpOut asserts a high when the DAC output voltage is equal to or greater than the Integrator output voltage.

14: In calibration modes, TEST resets the dark integration measurement, after which the first Calibration Clock (CalCLK) on FEED causes a dark integration measurement.

15: CalCLK causes an integration with IRED on, starting with the rising edge; it also increments the DAC input by 1 on the falling edge.

4.1.1 PROGRAMMING IN THE TYPICAL APPLICATION

Figure 4-1 shows the typical application circuit with special probe pads for test modes. Logic Inputs are FEED, IO, TEST2, and TEST. They all need to have driven inputs on these nodes in the test modes. TESTOUT is a digital output. RLED, and GLED are analog outputs.

Weak signals may be multiplexed to the RLED and GLED outputs. When this occurs, it is important to ground the anodes of D4 and D5 so that they are not overdriven by the current through the LEDs.

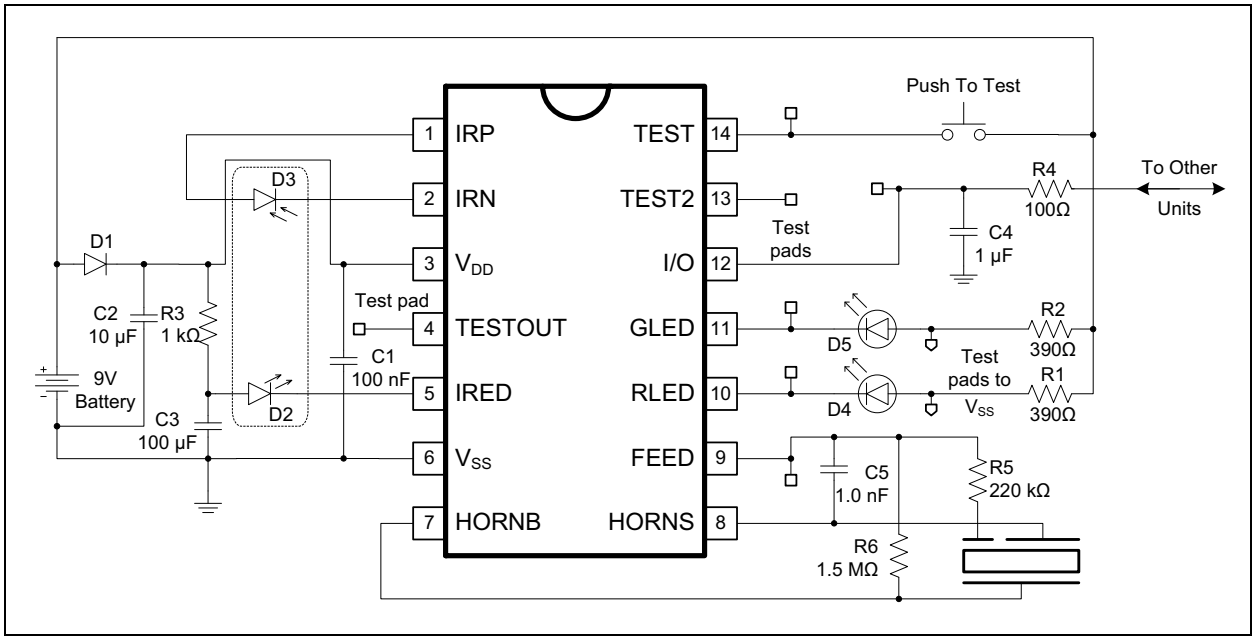


FIGURE 4-1: *Nominal Application Circuit for Programming.*

4.2 Horn Test (TM0)

Test mode TM0 allows the horn to be enabled indefinitely for audibility testing.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, TEST = IO = FEED = TEST2 = V_{SS}.
2. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0; the horn will be enabled.

In TM0, the TEST pin is the HornEnB control. To prevent the horn from sounding in TM0, TEST can be driven high. To prevent the horn from sounding while entering TM0, TEST may be driven high concurrently or just before TEST2 is driven to V_{DD}.

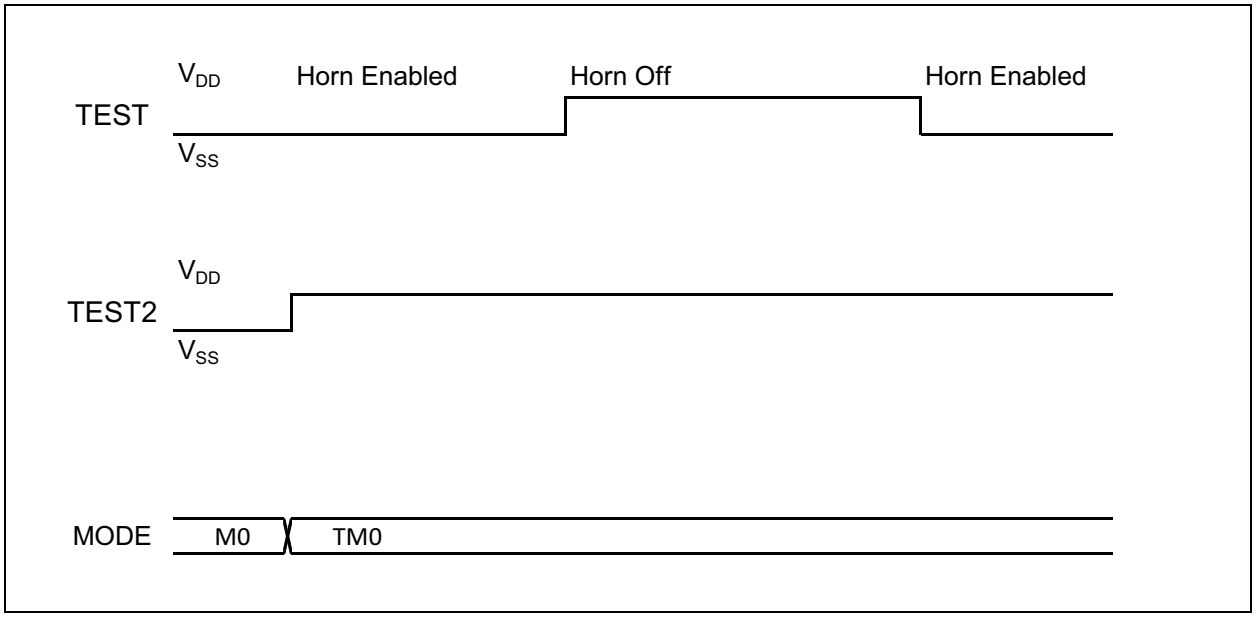


FIGURE 4-2: *Timing Diagram for Horn Test in Mode TM0.*

4.3 Serial Read/Write (TM1)

The feature selections and calibration values can be programmed in through the Serial Read/Write mode. Data is serially loaded into a shift register which is then used to program the EEPROM. All 60 bits must be loaded. This means temporary alarm limits and LTD values must be loaded if these values are not known. Calibration and LTD test modes can be used to update these values.

To enter test mode TM1 follow these steps:

1. Power up with the bias condition shown in Figure 4-1 to enter M0. At power-up, the 4 input pins TEST = IO = FEED = TEST2 = V_{SS}. TESTOUT is the serial output.
2. Drive the TEST2 input from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive the TEST input from V_{SS} to V_{DD} and hold at V_{DD}.
4. Apply one clock pulse to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM1. This enables the Serial Read/Write mode.
5. TEST now acts as a data input (1 = V_{DD}, 0 = V_{SS}) and FEED acts as the clock input (1 = V_{DD}, 0 = V_{SS}). Data is clocked in on the rising edge.
6. Shift in 60 bits of the user configuration and calibration settings. These settings are described in Register 4-1.
7. After the data has been entered into the shift register, pulse IO high for a minimum of 10 ms to store the data in EEPROM. The timing diagram is shown in Figure 4-3.
8. When test mode TM1 is entered, the contents of EEPROM are loaded into the shift register. The shift register contents are read out on TESTOUT as data is clocked in. If IO is not pulsed, the contents of the EEPROM are not changed.

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

				R/W	R/W	R/W	R/W
				LTDM5	LTDM4	LTDM3	LTDM2
				bit 59			bit 56

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LTDM1	LTDM0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
bit 55							bit 48

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	HUL5	HUL4
bit 47							bit 40

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HUL3	HUL2	HUL1	HUL0	HYL5	HYL4	HYL3	HYL2
bit 39							bit 32

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HYL1	HYL0	NL5	NL4	NL3	NL2	NL1	NL0
bit 31							bit 24

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LTDEn	IIRED2	IIRED1	TIRON2	TIRON1	GF2	GF1	LBTR1
bit 23							bit 16

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LBTR1	EOLEn	COEn	NoAAL	SyncEn	LBHshEn	AMHCEn	AMLEDn
bit 15							bit 8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AMTO2	AMTO1	AMEn	ShrtTO	SmrtH	HIAO	HushEnB	TSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 59-54 **LTDM<5:0>:** Long Term Drift Max Limit (**Section 3.3 "Photo Chamber Long Term Drift (LTD) Adjust"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

bit 53-48 **LTD<5:0>:** Long Term Drift Baseline (**Section 3.3 "Photo Chamber Long Term Drift (LTD) Adjust"**)
000000 = 0
000001 = 1
•
•
•
111110 = 62
111111 = 63

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

bit 47-42	**CTL<5:0>:** Chamber Test Limit (**Section 3.4 "Chamber Test"**) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 41-36	**HUL<5:0>:** Hush Limit (**Section 3.8 "Hush Timer Mode"**) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 35-30	**HYL<5:0>**: Hysteresis Limit (**Section 3.2 "Smoke Detection Circuitry"**) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 29-24	**NL<5:0>**: Normal Smoke Detection Limit (**Section 3.2 "Smoke Detection Circuitry"**) 000000 = 0 000001 = 1 • • • 111110 = 62 111111 = 63
bit 23	**LTDEn**: Long Term Drift Enable 1 = Enable 0 = Disable
bit 22-21	**IIRED<2:1>**: IRED Current Setting Select 00 = 50 mA 01 = 100 mA 10 = 150 mA 11 = 200 mA
bit 20-19	**TIRON<2:1>**: Integration Time Select 00 = 100 µs 01 = 200 µs 10 = 300 µs 11 = 400 µs
bit 18-17	**GF<2:1>**: Gain Factor Setting Select 00 = 1x 01 = 2x 10 = 4x 11 = 8x
bit 16-15	**LBTR<2:1>**: Low Battery Trip Point Select 00 = 7.5V 01 = 6.9V 10 = 7.8V 11 = 7.2V
bit 14	**EOLEn**: End-of-Life Indicator Enable 1 = Enable 0 = Disable

REGISTER 4-1: USER CONFIGURATION SETTINGS AND CALIBRATION SETTINGS

bit 13	**COEn**: CO Alarm Function (Smart IO) Enable 1 = Enable 0 = Disable
bit 12	**NoAAL**: Auto Alarm Locate Disable 1 = AAL is disabled 0 = AAL is enabled
bit 11	**SyncEn**: Horn Synchronization Enable 1 = Enable 0 = Disable
bit 10	**LBHshEn**: Low-Battery Hush Enable 1 = Enable 0 = Disable
bit 9	**AMHCEn**: Alarm Memory PTT Indicator Horn Chirp Enable 1 = Enable 0 = Disable
bit 8	**AMLEDEn**: Alarm Memory PTT Indicator LED Flashing Enable 1 = Enable 0 = Disable
bit 7-6	**AMTO<2:1>**: Alarm Memory Standby LED indicator Time Out Select 00 = 24 hour 01 = 48 hour 10 = 0 11 = never time out
bit 5	**AMEn**: Alarm Memory Enable 1 = Enable 0 = Disable
bit 4	**ShrtTO**: Hush Timer Time Out Select 1 = 80s 0 = 9 minutes
bit 3	**SmrtH**: Smart Hush Enable 1 = Enable (Hush is canceled by either high smoke or remote smoke) 0 = Disable (Hush is never canceled until time out)
bit 2	**HIAO**: Hush-in-Alarm-Only Enable 1 = Enable (Hush is activated upon release of PTT during local alarm only) 0 = Disable (Hush is activated upon release of PTT at anytime)
bit 1	**HushEnB:** Hush Enable 1 = Hush is disabled 0 = Hush is enabled
bit 0	**TSEL:** Horn Select 1 = Continuous Horn Pattern 0 = Temporal Horn Pattern

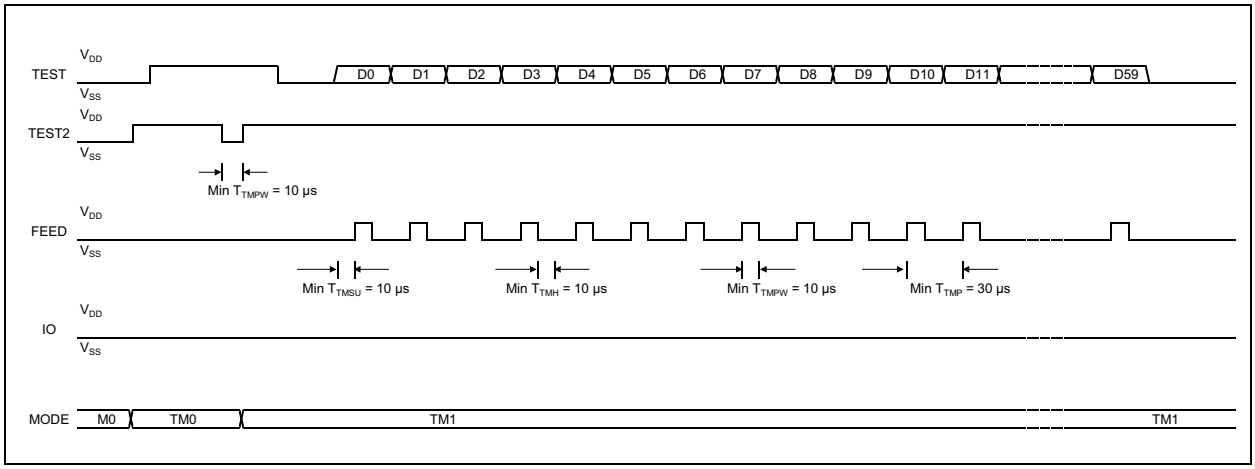


FIGURE 4-3: *Timing Diagram for User Feature Selection in Serial Read/Write Mode TM1.*

4.4 Low Battery Test (TM2)

Test mode TM2 allows the low battery trip point to be tested.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, TEST = IO = FEED = TEST2 = V_{SS}.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.
4. Apply two clock pulses to the TEST2 input (V_{DD} to V_{SS} and then back to V_{DD}) to enter in TM2 mode.
5. Drive IO from V_{SS} to V_{DD} to enable the low battery testing and turn on the RLED. Sweep V_{DD} from high to low and monitor TESTOUT output. The TESTOUT output will indicate the low battery status (High = low battery detected).

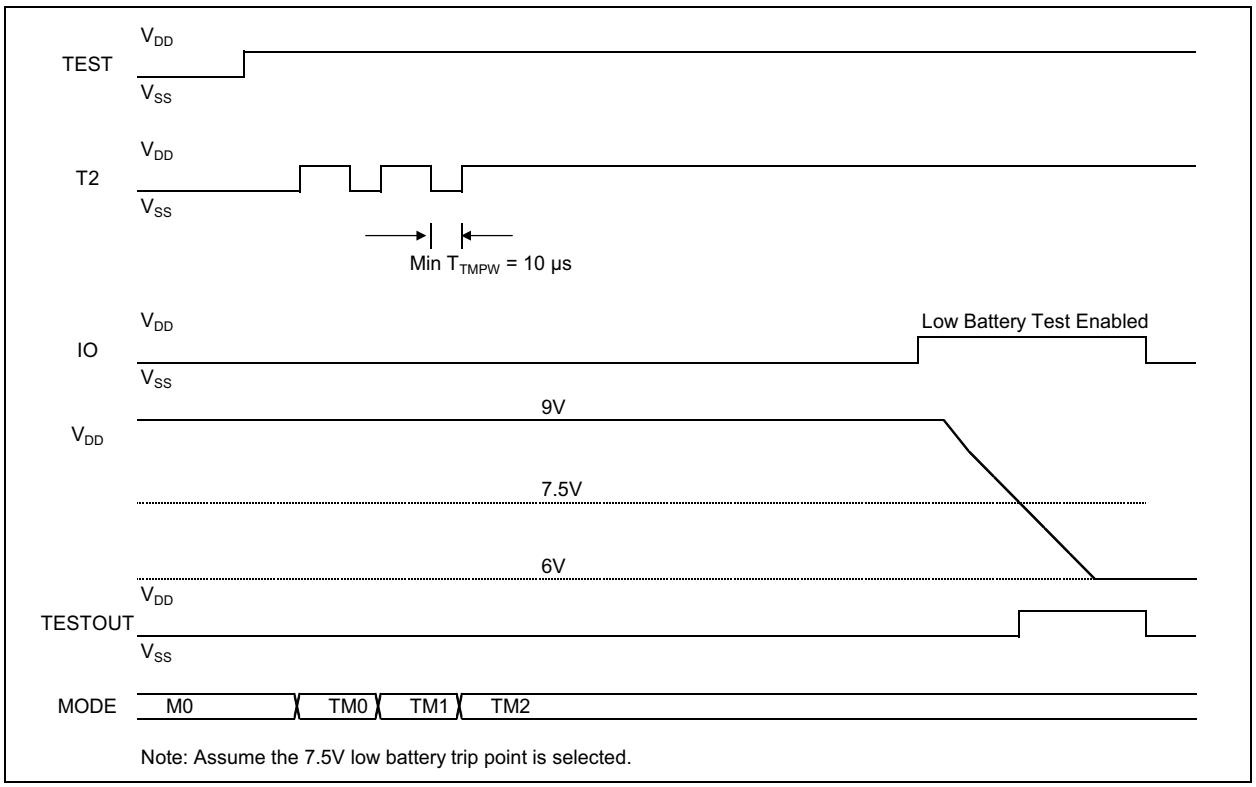


FIGURE 4-4: *Timing Diagram for Low Battery Test in Mode TM2.*

4.5 End-Of-Life Serial Read/Write (TM3)

The 10-year End-of-Life feature can be read and modified through the TM3 Serial Read/Write mode. This allows for the possibility of setting shorter End-of-Life values for different applications, such as three or five years. Note that the controls for data, clock, and program are the same as the previous Serial Read/Write mode, but a different register is used.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, drive four input pins (probe pads) TEST = IO = FEED = TEST2 = V_{SS}. TESTOUT, RLED, and GLED are outputs and should not be driven.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.
4. Apply three clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter in TM3. This enables the EOL Serial Read/Write mode.
5. Drive TEST low to V_{SS}.
6. TEST acts as a data input (`1` = V_{DD}, `0` = V_{SS}).
7. TESTOUT acts as the data output (`1` = V_{DD}, `0` = V_{SS}).
8. FEED acts as the clock input (`1` = V_{DD}, `0` = V_{SS}).
9. Data is clocked on the rising edge.
10. Shift in the values of the eight EOL bits, MSB first.
11. Drive IO high for 10 ms to program the new EOL counter value.

REGISTER 4-2: END-OF-LIFE REGISTER

W	W	W	W	W	W	W	W
EOL0	EOL1	EOL2	EOL3	EOL4	EOL5	EOL6	EOL7
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 0-7 **EOL<0:7>:** Long Term Drift Max Limit (**Section 3.10 "End-of-Life (EOL) Indicator"**)

```
00000000 = 0
10000000 = 1
•
•
•
01111111 = 254
11111111 = 255
```

4.5.1 END-OF-LIFE EXAMPLE

For a 10-year EOL timeout, the internal counter counts up to 241 clocks incremented every 364 hours (≈15days). The counter starts at zero. To shorten the EOL timeout, the EOL register can be loaded with a non-zero value.

For a 7-year EOL timeout, start with EOL value of 72 instead of 0. Table 4-4 shows the bit settings for a 7-year EOL.

TABLE 4-4: SEVEN-YEAR EOL

Data	0	0	0	1	0	0	1	0
Bit #	0	1	2	3	4	5	6	7
Value	0	0	0	8	0	0	64	0

When the part reaches a count of 241, the EOL warning will occur. In this 7-year example, the starting value was 72, so the clock will be incremented 169 (241-72) times, for a total of 169 x 364 hours, or 61516 hours, or 7.0 years.

4.6 Limits Verification (TM4, TM5, TM6, TM7)

After the RE46C200 has been configured, test modes are available to verify that the limits are functioning as expected. Table 4-5 describes the limit verification test modes. These test modes are ordered to facilitate smoke box verification, going from no smoke, to minimum smoke, to maximum no smoke alarm (hysteresis), to minimum Hush smoke. Overall, this means starting with no smoke and ending with maximum smoke.

To enter these test modes, follow these steps:

1. Power up with the bias condition shown in Figure 4-1 to enter M0. At power-up, the four input pins TEST = IO = FEED = TEST2 = V_{SS}. TESTOUT, RLED, and GLED are outputs that are used to monitor the system response.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD}.
4. Apply four clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM4.
5. With appropriate smoke level in chamber, pull TEST low to V_{SS}, and then drive FEED to V_{DD} for at least 2 ms. TESTOUT will indicate detection status (HIGH = detection). The integrator and DAC voltages can be monitored on the GLED and RLED pins, respectively.
6. Drive TEST high to V_{DD} and clock TEST2 once. This places the RE46C200 in the next test mode.
7. Repeat Steps 5 and 6 above until each verification mode has been checked.

This operation causes a dark (IRED off) measurement followed by a lit (IRED on) measurement. The difference is digitized and compared to the 6-bit alarm limit. The resulting compare comes out on TESTOUT. A logic high is output as soon as the measurement digitization exceeds the smoke alarm limit.

Figure 4-5 shows the timing diagram for the Limits Verification procedure.

TABLE 4-5: ALARM LIMITS VERIFICATION DESCRIPTION

Function	Mode	TEST2 Clocks (Low, then High)
PTT/Chamber Test	TM4	Clock TEST2 4x
Standby	TM5	Clock TEST2 5x
Hysteresis	TM6	Clock TEST2 6x
Hush	TM7	Clock TEST2 7x

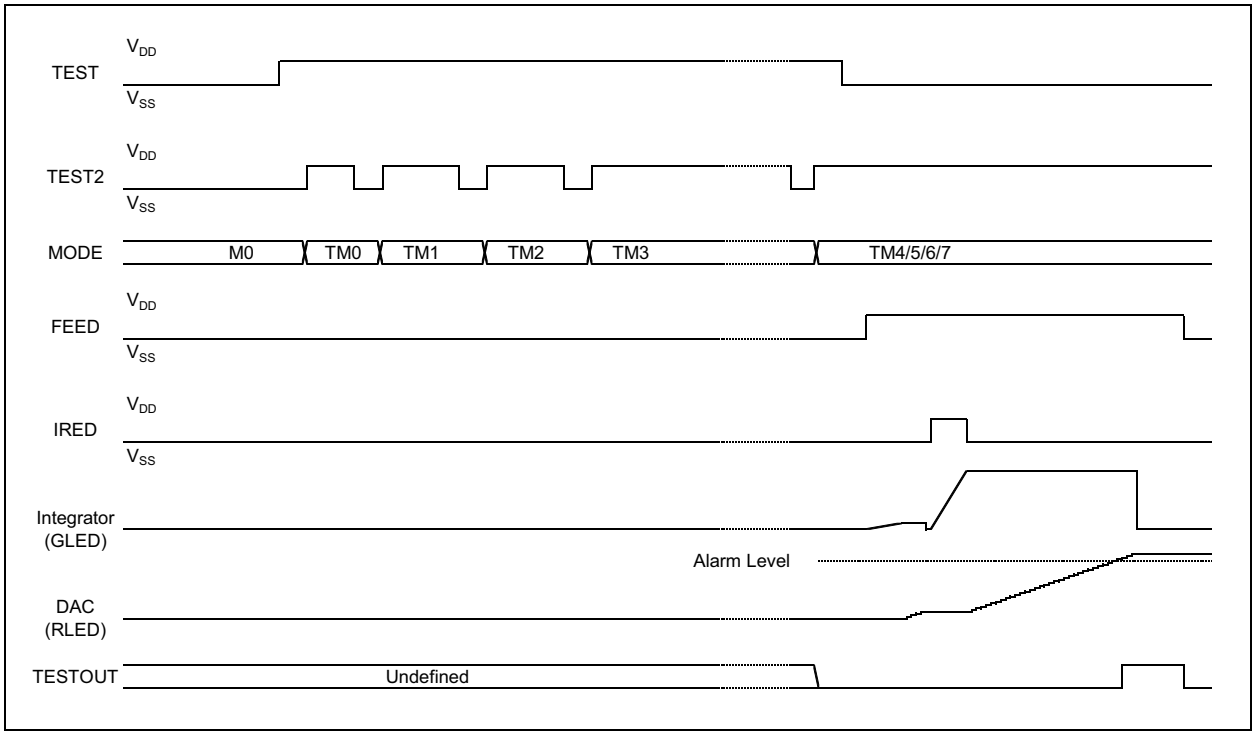


FIGURE 4-5: *Timing Diagram for Limit Verification in Mode TM4 ~ TM7.*

4.7 Long Term Drift Calibration (TM10, TM11)

Measurement and programming of the long term drift baseline value is done in test modes TM10 and TM11, respectively. Alternately, in a well-characterized system, TM1 may be used to program LTD and LTD_{max} without measurement. LTD_{max} must be set to a value greater than the LTD value.

4.7.1 BASELINE LTD MEASUREMENT (TM10)

To enter this mode, follow these steps:

1. Power up with the bias condition shown in Figure 4-1 to enter M0. At power-up, drive four input pins (probe pads) TEST = IO = FEED = TEST2 = V_{SS}. TESTOUT, RLED, and GLED are outputs that are used to monitor the system response.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD}.
4. Apply ten clock pulses to the TEST2 input (V_{DD} to V_{SS} and back to V_{DD}) to enter TM10.
5. Drive TEST from V_{DD} to V_{SS} before measuring.
6. Driving FEED high for at least 2 ms causes a baseline dark (IRED off) measurement followed by a lit (IRED on) measurement. The difference is digitized and accumulated to the LTD counter. The integrator and DAC voltages can be monitored on the GLED and RLED pins, respectively. The comparison of the DAC and the integrator voltages comes out on the TESTOUT pin.
7. The baseline LTD value that is held in the LTD counter is latched into the programming register by clocking IO while TEST and FEED are low.
8. The LTD value is stored in EEPROM in TM11.
9. In order to set the LTD_{max} value, the value held in the LTD counter can be incremented by pulsing TEST from V_{SS} to V_{DD} and back to V_{SS}. Each pulse increments the LTD counter by one.
10. The LTD_{max} value held in the LTD counter is latched into the programming register by clocking IO while TEST is high and FEED is low.

4.7.2 LTD PROGRAMMING (TM11)

After the LTD and LTD_{max} values are latched in the programming register in TM10, values may be programmed into EEPROM in TM11.

1. To enter LTD programming mode TM11, with TEST high and clock TEST2 once from TM10.
2. Drive TEST to V_{SS}.
3. Pulse IO to V_{DD} for 10 ms minimum.
4. The LTD and LTD_{max} values are now stored in EEPROM.

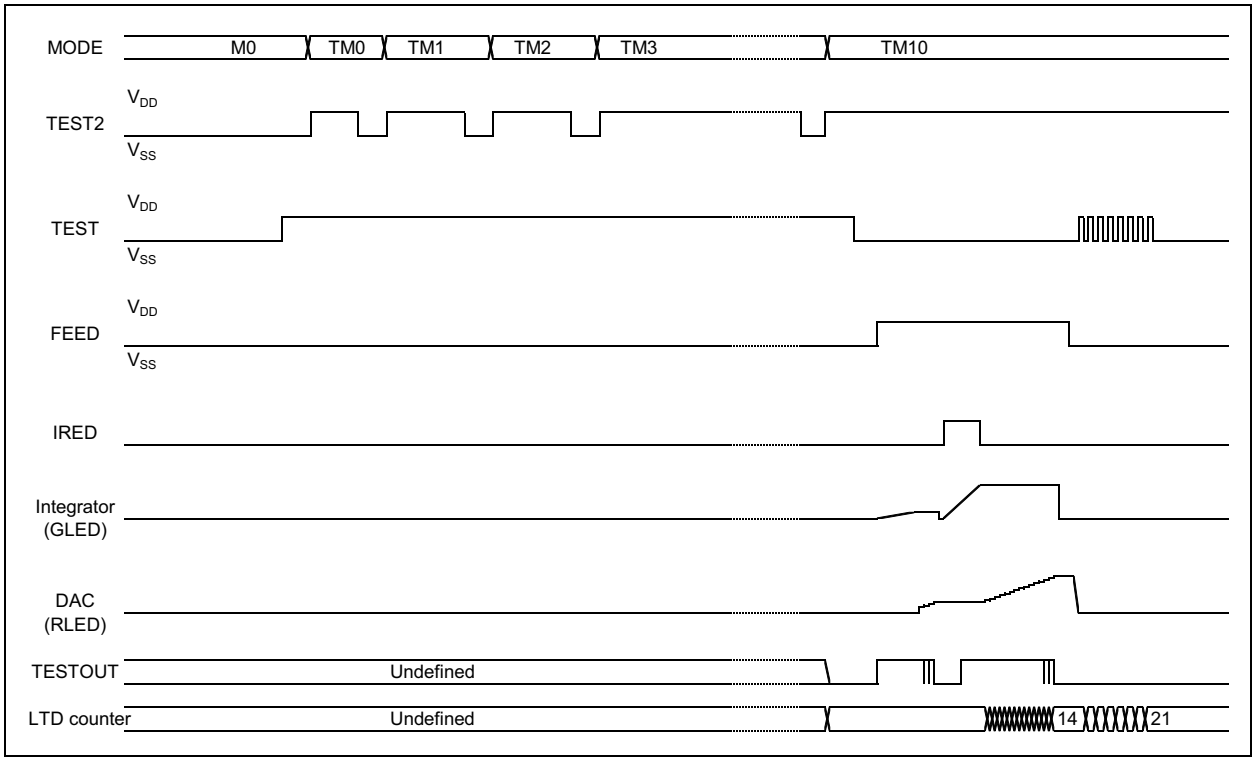


FIGURE 4-6: *Timing Diagram for LTD Calibration Mode in TM10.*

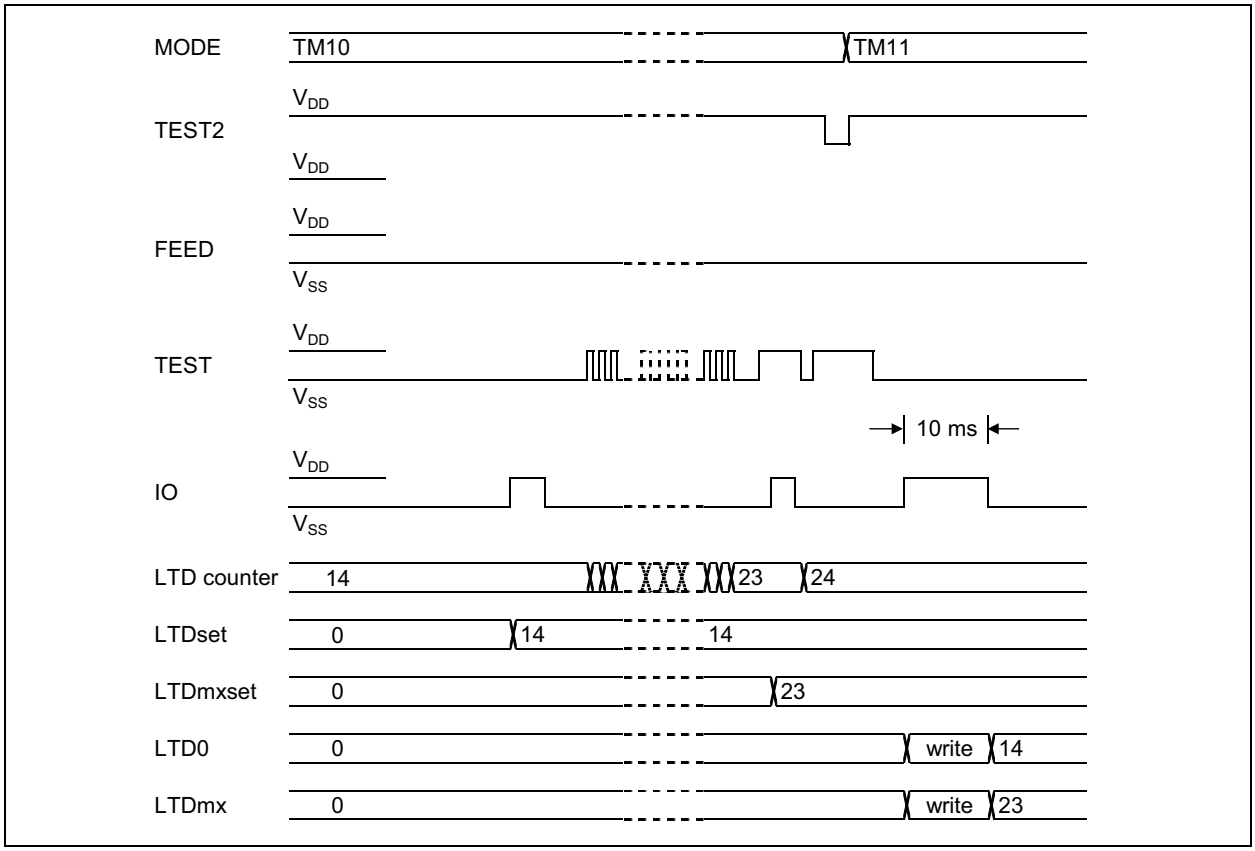


FIGURE 4-7: *Timing Diagram for LTD Calibration Setting and Programming in Modes TM10 ~ TM11.*

4.8 Smoke Calibration (TM12, TM13, TM14, TM15)

A separate calibration test mode is used for each measurement mode (PTT/Chamber Test, Normal, Hysteresis, and Hush) so that alarm limits can be set for each.

The calibration test modes are listed in Table 4-6. In all calibration test modes, the integrator output can be accessed at the GLED output. The DAC output voltage, which represents the smoke detection level, can be accessed at the RLED output and the comparator output can be accessed at TESTOUT.

The FEED input is clocked to step up the smoke detection level at RLED. Each FEED clock increments the DAC and initiates a smoke measurement. When the smoke detection level is less than the photo amp output voltage, TESTOUT will be asserted high. When the smoke detection level is equal to or greater than the photo amp output voltage, TESTOUT will remain low. To save this smoke alarm limit, the IO input is pulsed low-to-high to store the result in the programming register. In TM15, when the IO is pulsed, the result is stored in the programming register and then all four results in the programming register are programmed into the EEPROM. The IO pulse in TM15 should be at least 10 ms.

TABLE 4-6: ALARM LIMIT CALIBRATION MODES

Alarm Limit	Mode	TEST2 Clocks (Low, then High)
PTT/Chamber Test	TM12	Clock TEST2 12x
Standby Alarm Limit	TM13	Clock TEST2 13x
Hysteresis Alarm Limit	TM14	Clock TEST2 14x
Hush Alarm Limit	TM15	Clock TEST2 15x

4.8.1 SIMPLE ALARM LEVEL CALIBRATION

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, drive four input pins (probe pads) TEST = IO = FEED = TEST2 = V_{SS}. TESTOUT, RLED, and GLED are outputs that are used to monitor the system response.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD}.
4. To calibrate an alarm limit setting, clock TEST2 to the test mode (TM12, TM13, TM14, and TM15 as indicated above).
5. With appropriate smoke level in chamber, pull TEST low to V_{SS}, and then drive FEED to V_{DD} and hold at least for 2 ms. The integrator and DAC voltages come out on the GLED and RLED pins, respectively. This operation causes a baseline dark (no IRED) measurement followed by a lit (IRED) measurement.
6. Clock FEED (hold FEED high for at least 2 ms) until TESTOUT no longer transitions high after an integration. Unlike the Limit Verification, digitization does not occur automatically, but instead the DAC is incremented on each falling edge of FEED. The DAC voltage is shown on the RLED pin. When the DAC output is greater than the integrator output, TESTOUT will not transition high. Then, with FEED held low, pulse IO high for 10 µs to latch the data into the programming register.
7. To store the TM15 limit and program all the alarm limits in to EEPROM, pulse IO high for 10 ms.

4.8.2 QUICKER ALARM LEVEL CALIBRATION

FEED can be used to skip tests below the minimum alarm level.

1. To calibrate a smoke detection level, clock TEST2 to the test mode (TM12, TM13, TM14, and TM15 as indicated above).
2. With appropriate smoke level in chamber, pull TEST low to V_{SS}, then drive FEED to V_{DD} and hold for at least 2 ms, for the first full integration. The integrator and DAC voltages come out on the GLED and RLED pins, respectively. This operation causes a baseline dark (no IRED) measurement followed by a light (IRED) measurement.
3. Clock FEED high for 5 µs with a 10 µs period until the minimum of the calibration range is reached then hold FEED low for greater than 2 ms.
4. Clock FEED high for at least 2 ms until TESTOUT no longer transitions high after an integration.

4.8.3 DECREMENTING ALARM LIMIT CALIBRATION

If the desired alarm limit is one step below the measured alarm limit, the measurement can effectively be decremented. The measurement counter rolls over at 64, so incrementing FEED 63 times is equivalent to decrementing the measurement by 1.

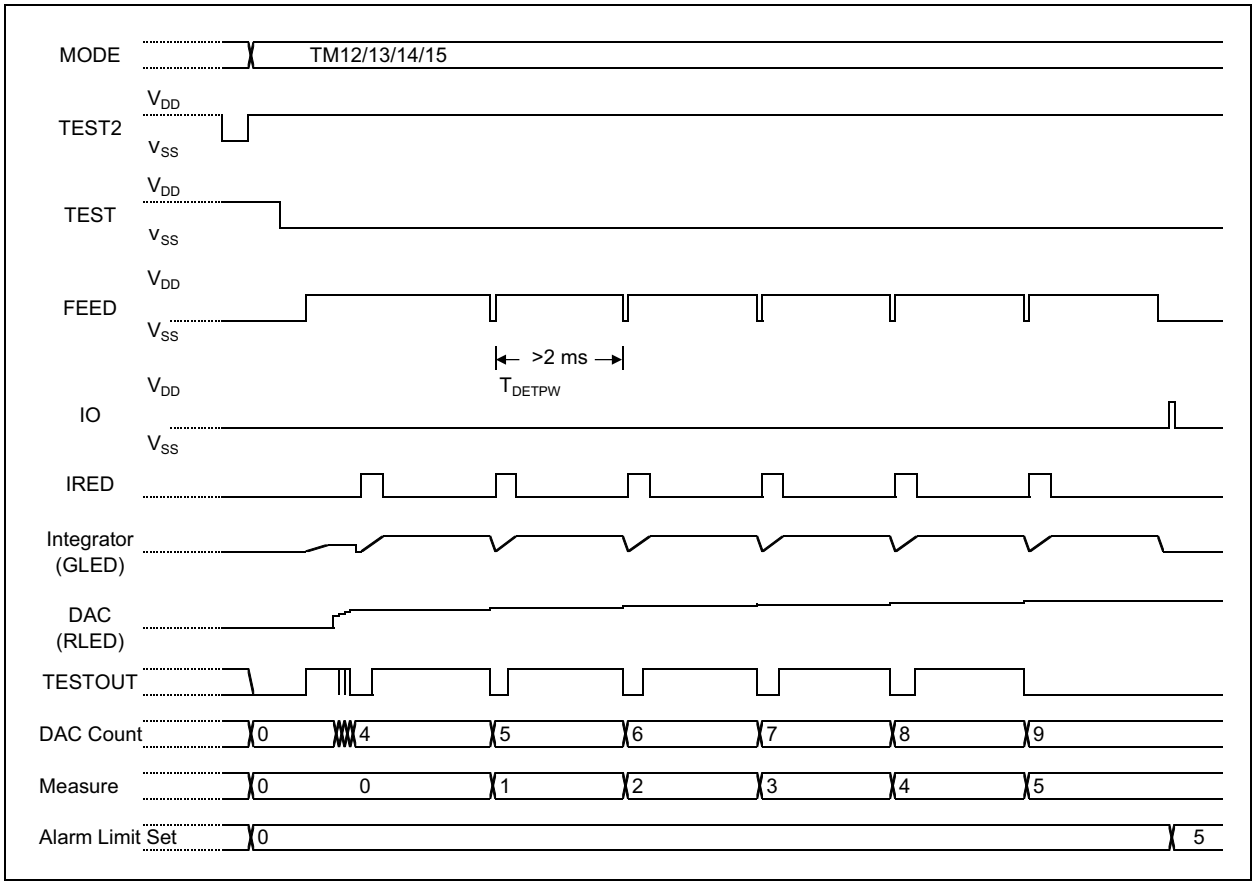


FIGURE 4-8: *Timing Diagram for Simple Alarm Limit Calibration in Mode TM12 ~ TM15.*

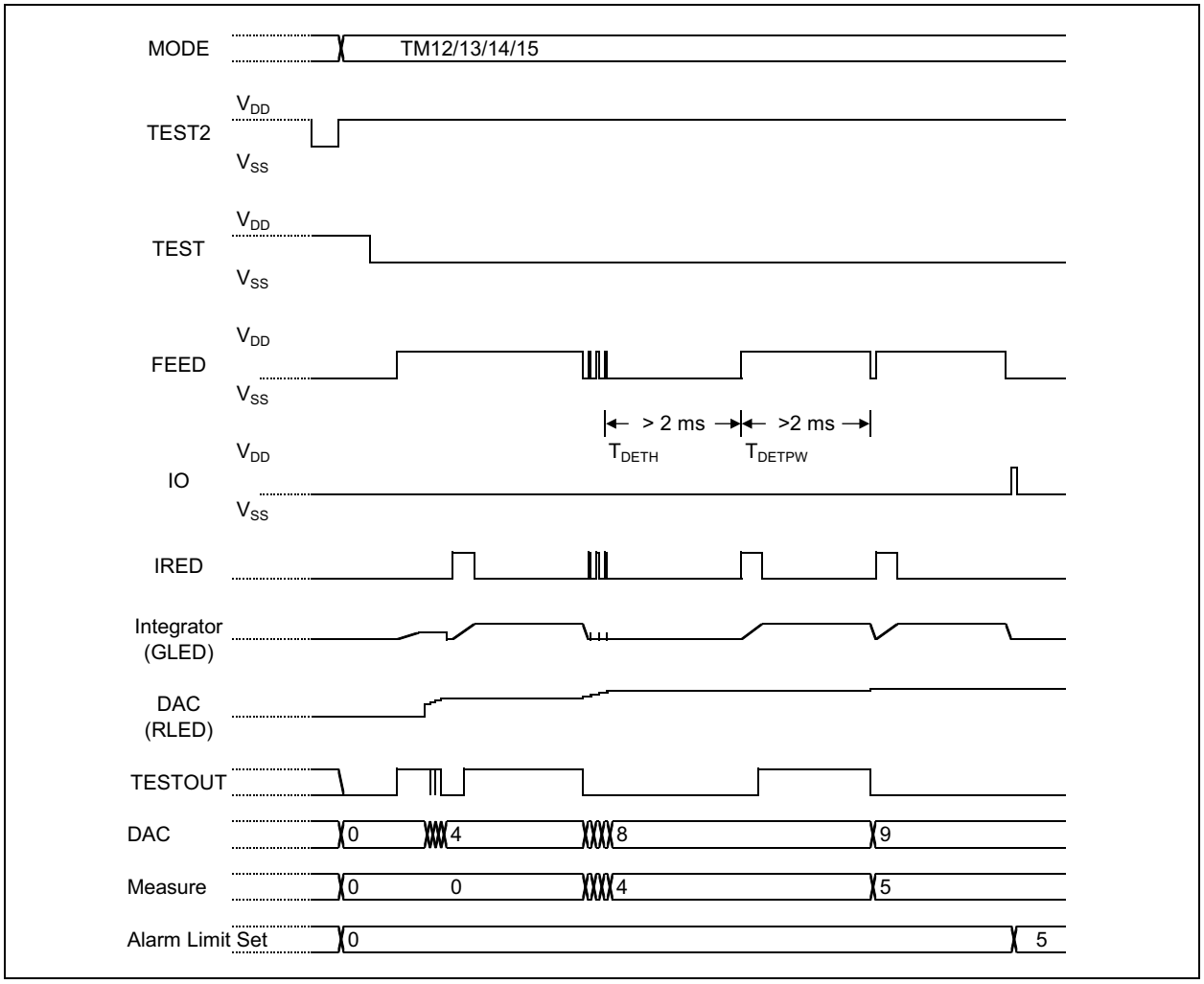


FIGURE 4-9: *Timing Diagram for Quick Alarm Limit Calibration in Mode TM12 ~ TM15.*

4.9 Lock Bit Programming (TM19)

Test mode TM19 allows users to program the EE lock bit. Once the EE lock bit is set, the programmed user EE data cannot be changed, unless the lock bit is reset.

To enter this mode, follow these steps:

1. Power-up with the bias condition shown in Figure 4-1 to enter M0. At power-up, TEST = IO = FEED = TEST2 = V_{SS}.
2. Drive TEST from V_{SS} to V_{DD} and hold at V_{DD}.
3. Drive TEST2 input from V_{SS} to V_{DD} and hold at V_{DD} to enter TM0.
4. Apply 19 clock pulses to the TEST2 input (V_{DD} to VSS and then back to V_{DD}) to enter in TM19 mode.
5. Hold TEST at V_{DD} and pulse IO once to set the lock bit and store it into EEPROM memory.
6. To reset the lock bit, in step 5, drive TEST to V_{SS} and pulse IO once to reset the lock bit.

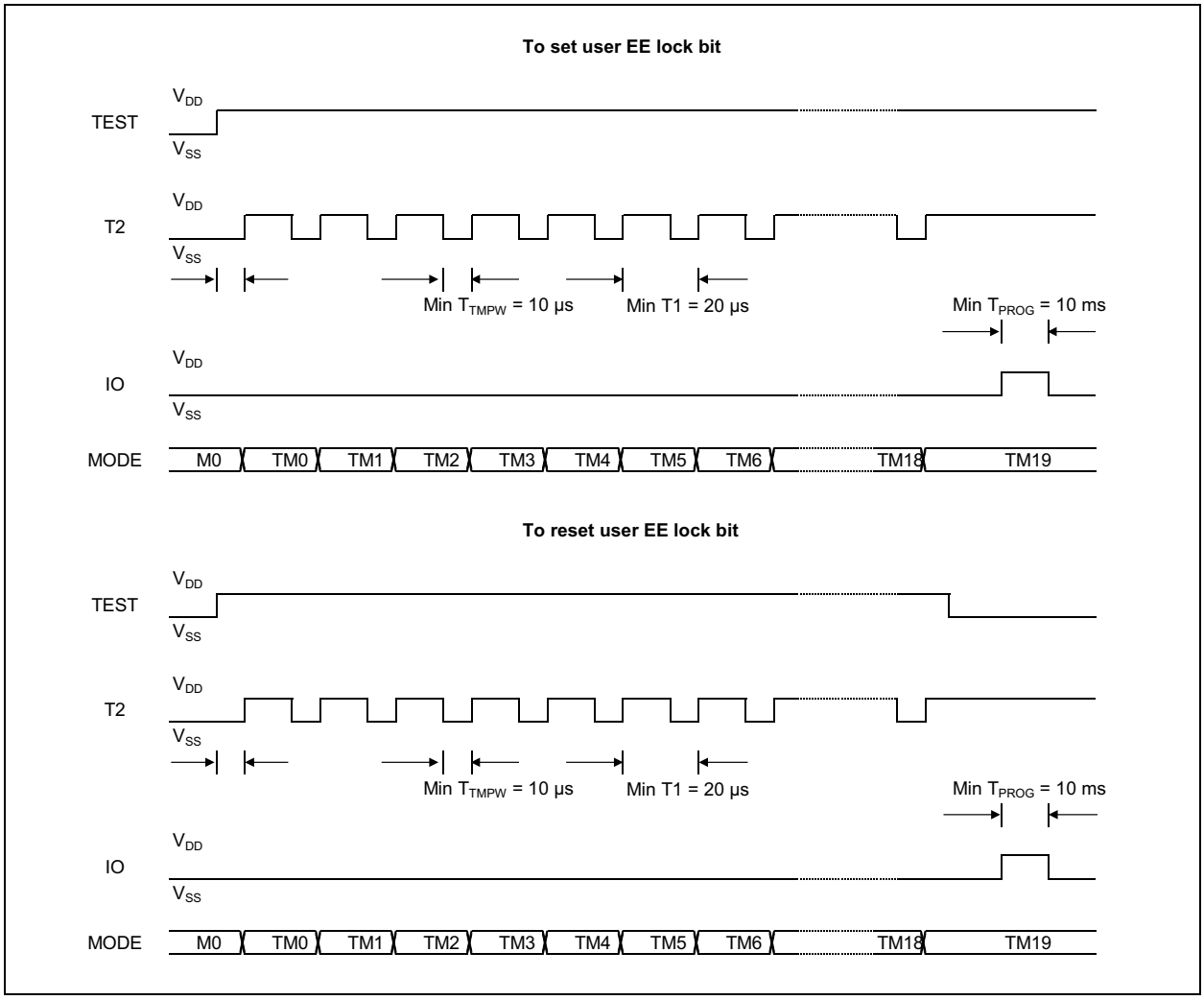


FIGURE 4-10: *Timing Diagram for User Lock Bit Programming in Mode TM19.*

NOTES:

5.0 APPLICATION NOTES

5.1 Standby Current Calculation

A calculation of the standby current is shown in Table 5-1, which is based on the Typical Application and the following conditions:

V_{DD}	=	9V
LED current in loaded battery check (V_{fLED}=2.0V, V_{DS}=0.5V, R1 = 390)	=	16.7 mA
End-of-Life enabled		(EOLEn = 1)
Detection Integration Time	=	220 µs
IRED Current	=	200 mA

TABLE 5-1: STANDBY CURRENT CALCULATION

I_{DD} Component	Current (µA)	Duration (s)	Period (s)	Duty Cycle	Average Current (µA)
Fixed I_{DD}	**0.9**	**Always**	**Always**	**1**	**0.9**
Photo Detection Current					
Smoke Detection					
Excluding IR drive	170	5.00E-03	10	500E-6	86E-3
IR drive during Detection	200E+3	220E-6	10	20E-6	4.4
Subtotal					**4.5**
Chamber Test					
Excluding IR drive	170	5.00E-03	320	16E-6	2.7E-3
IR drive during Detection	200E+3	220E-6	320	625E-9	138E-3
Subtotal					**140E-3**
Low Battery Check					
Unloaded	20	10E-3	80	125E-6	2.5E-3
Loaded	16.7E+3	10E-3	320	231E-6	522E-3
Subtotal					**524E-3**
End-of-Life					**5E-6**
				Total	**6.1**

The following sections explain the current components in Table 5-1.

5.1.1 FIXED IDD

This is the current draw from the internal oscillator, which is constantly running in normal operation.

5.1.2 SMOKE DETECTION

This is the current draw from the smoke detection circuitry during the 5 ms smoke check period. This is done every 10s in normal standby operation.

The IR drive component of smoke detection typically is the biggest factor in the overall smoke detector current budget. Careful selection of integration time and IRED current can maximize detector battery life.

For IR drive in Table 5-1, the setting of 200 mA and 220 µs was selected, which reflects an average of 4 µA.

Reducing the integration time or the IRED current will decrease the IR drive component proportionately. For example, halving the integration time from 220 µs to 120 µs will halve the average current from 4.4 µA to 2.2 µA; using a 100 µA IRED current and 100 µs integration time will reduce average current to 1.1 µA.

Likewise, increasing to maximum settings will increase the current draw. Using a 440 µs integration time and 200 mA IRED yields a maximum (nominal) average current draw of 8.8 µA.

5.1.3 CHAMBER TEST

This is the current draw from the smoke detection circuitry during the 5 ms chamber test. This is done every 320s in normal standby operation.

The integration time, IRED current and gain factor settings also apply to the chamber test. However, since the check is less frequent, the average current contribution is relatively small. At most, this test will add around 0.3 µA to the overall current budget.

5.1.4 LOW BATTERY CHECK (UNLOADED)

This is the current draw from the low battery detection circuitry during the 10 ms unloaded low battery check period.

5.1.5 LOW BATTERY CHECK (LOADED)

This is the current draw from the RLED during the 10 ms loaded low battery check period. The 16.7 mA current load is based on an LED forward diode voltage of 2.0V, a driver V_{DS}(on) = 0.5V and R1 = 390Ω. This current will degrade as the battery voltage drops, eventually reducing to around 12 mA at a low battery voltage of 7.2V.

Proper selection of battery test load is needed to adequately test for a low battery condition. Likewise, the selection of a low battery voltage is also important to ensure sufficient horn levels in alarm and battery life.

5.1.6 END-OF-LIFE

This is the current draw to read EOL bits from EE and then increase by 1, followed by writing the EOL bits back to EE. The average 5 pA cost of operating end-of-life is inconsequential to the overall current usage.

5.1.7 TOTAL CURRENT

This is the average total current draw in standby.

5.2 FUNCTIONAL TIMING DIAGRAMS

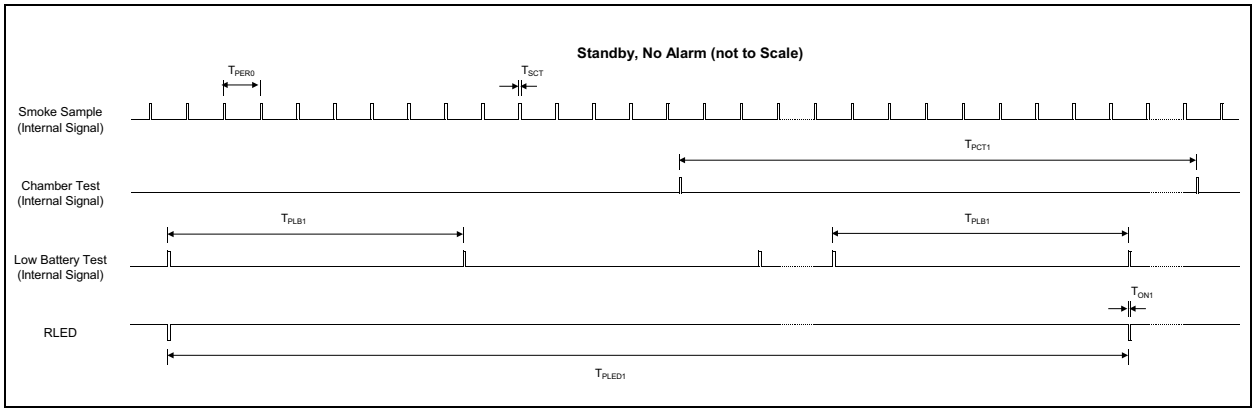


FIGURE 5-1: *Timing Diagram – Standby, No Alarm.*

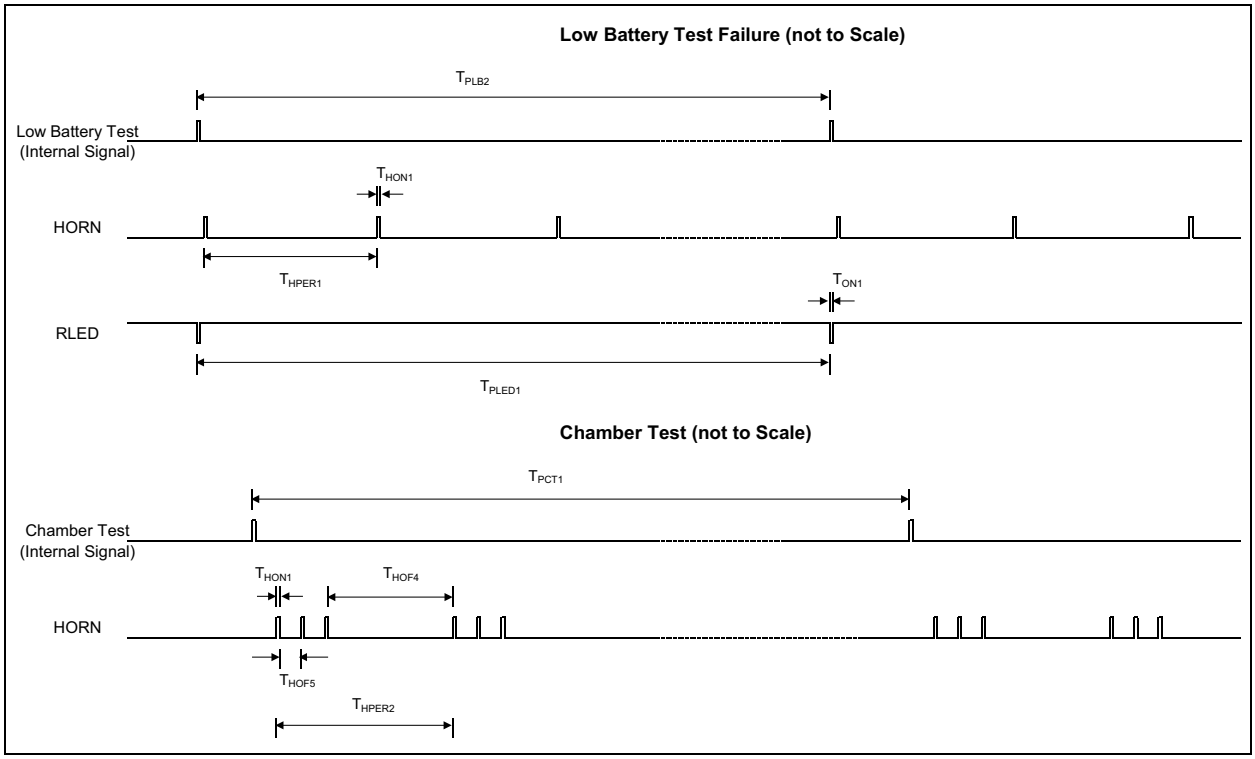


FIGURE 5-2: *Timing Diagram – Low Battery Test Failure and Chamber Test Failure.*

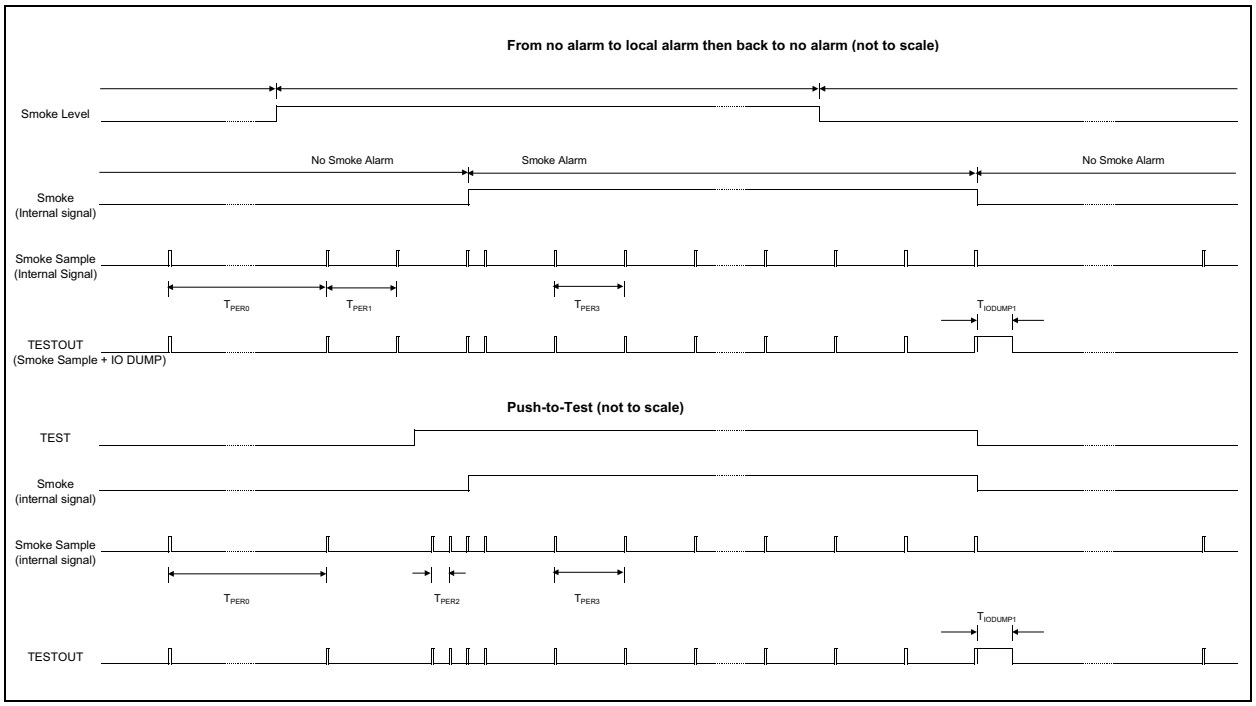


FIGURE 5-3: *Timing Diagram – From Standby to Local Smoke and Push-To-Test.*

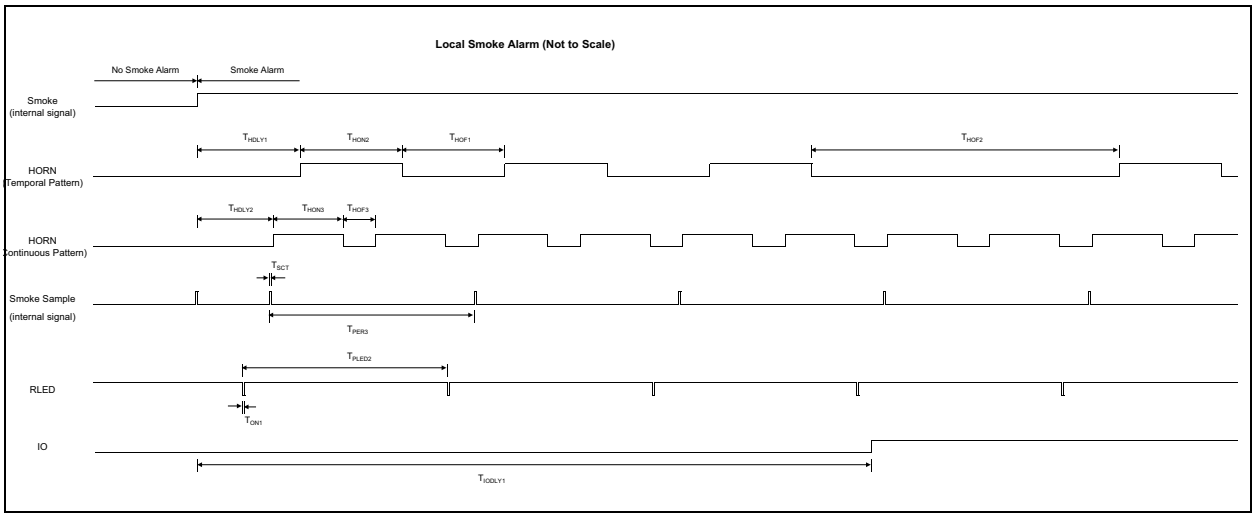


FIGURE 5-4: *Timing Diagram – Local Smoke Alarm.*

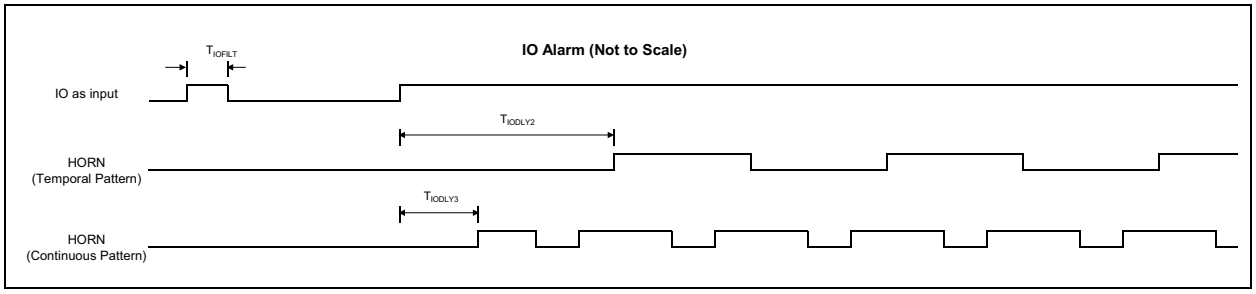


FIGURE 5-5: *Timing Diagram – IO Smoke Alarm.*

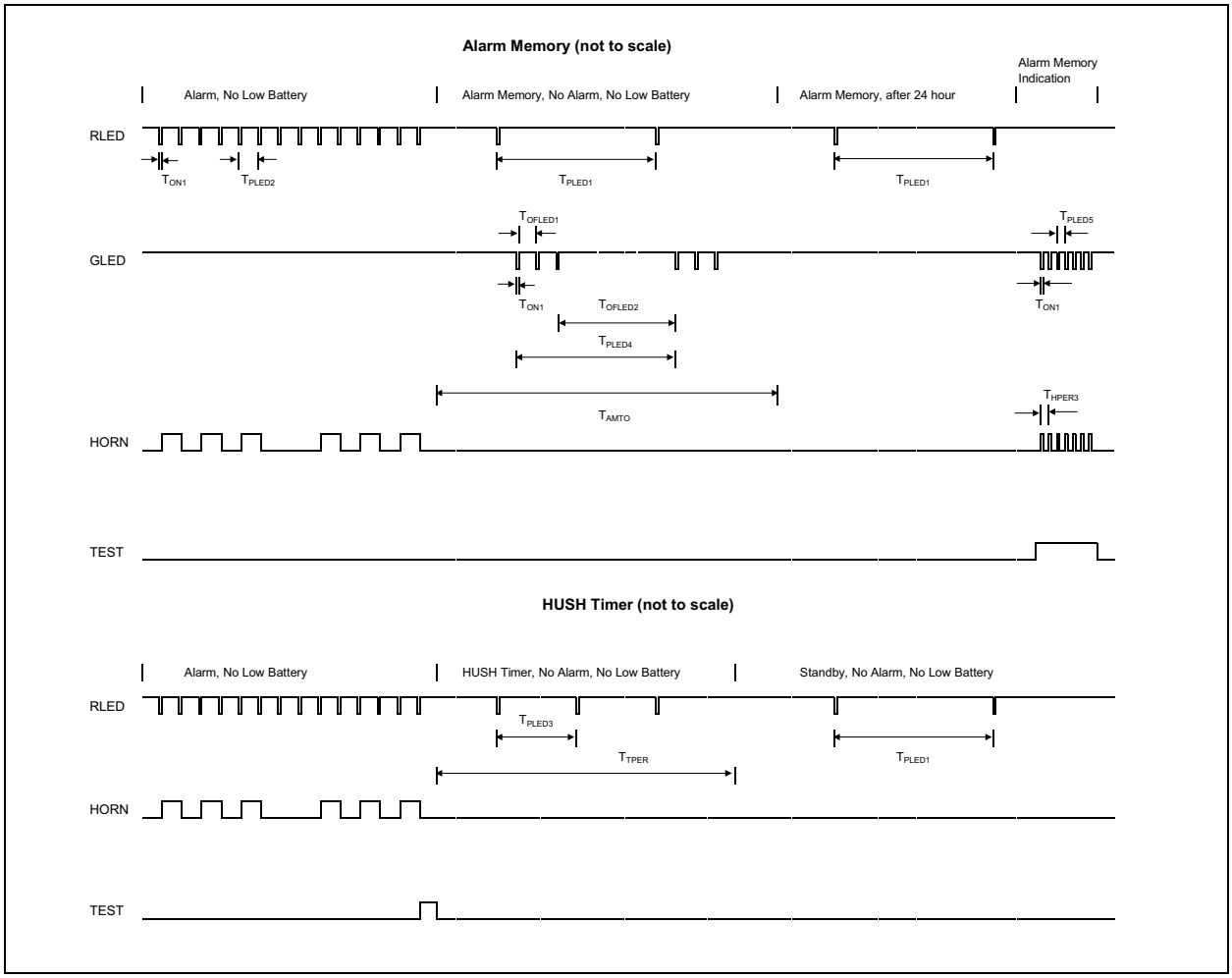


FIGURE 5-6: *Timing Diagram – Alarm Memory and Hush Timer.*

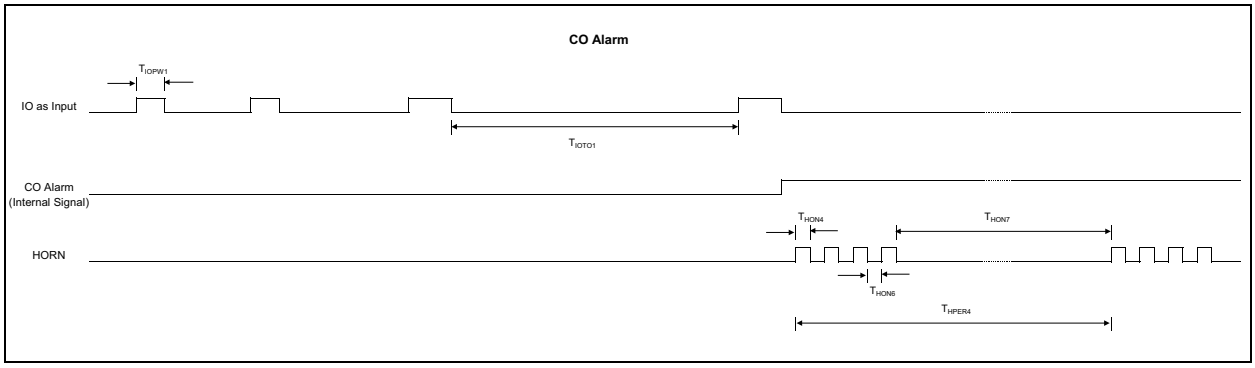


FIGURE 5-7: *Timing Diagram – CO Alarm.*

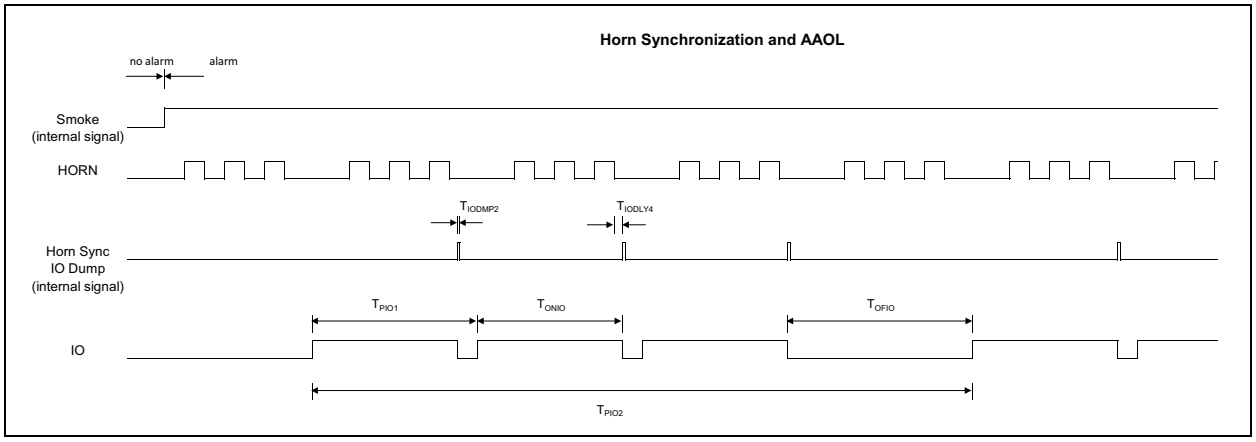
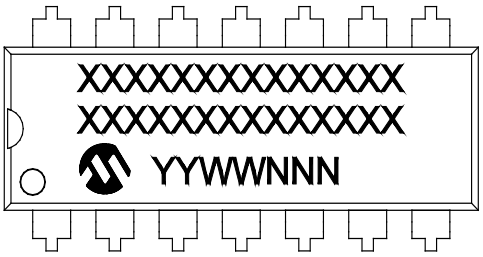


FIGURE 5-8: *Timing Diagram – Horn Synchronization and AAL.*

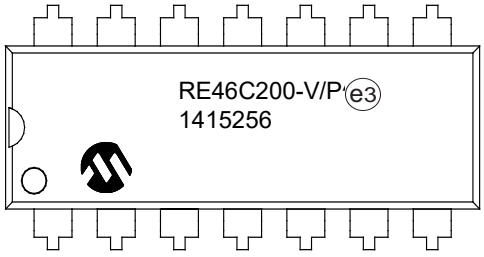
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

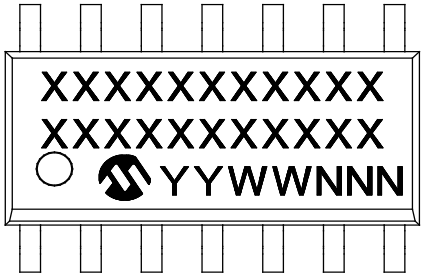
14-Lead PDIP (300 ml)



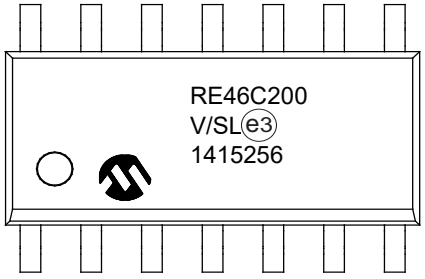
Example



14-Lead SOIC (3.90 mm)



Example

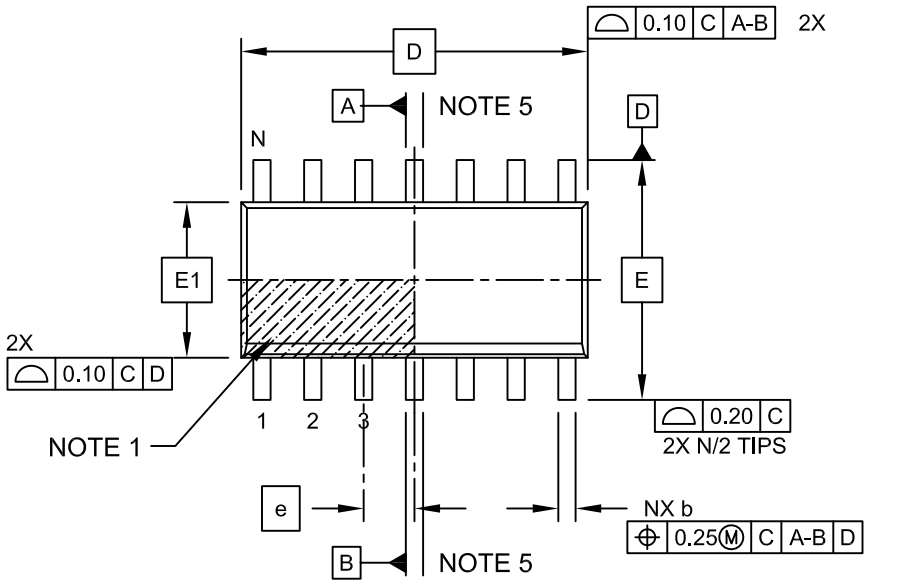


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

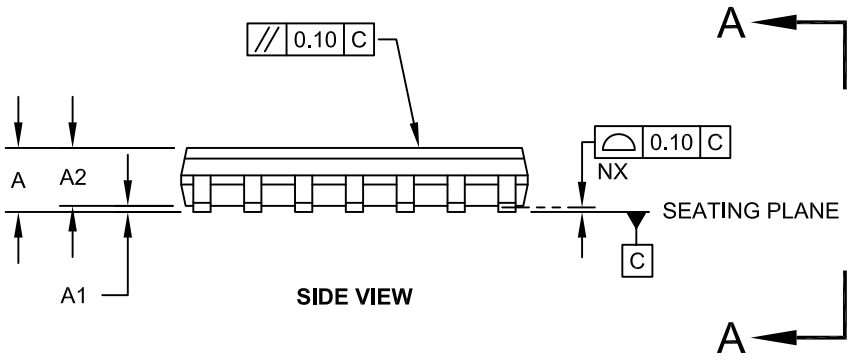
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

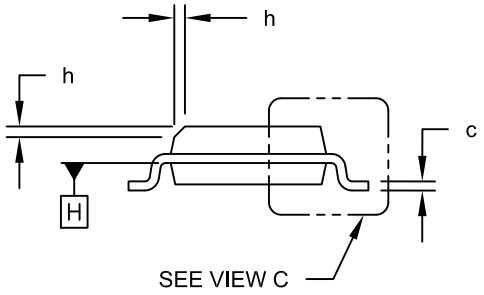
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

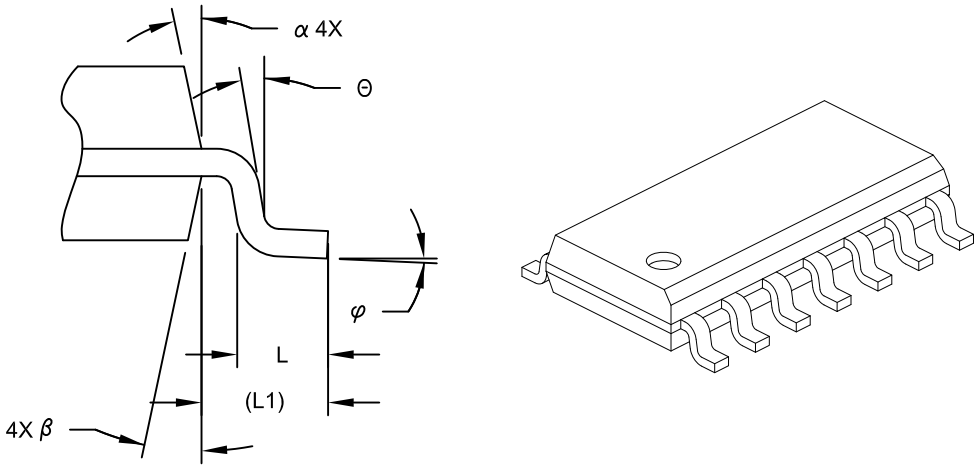


VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

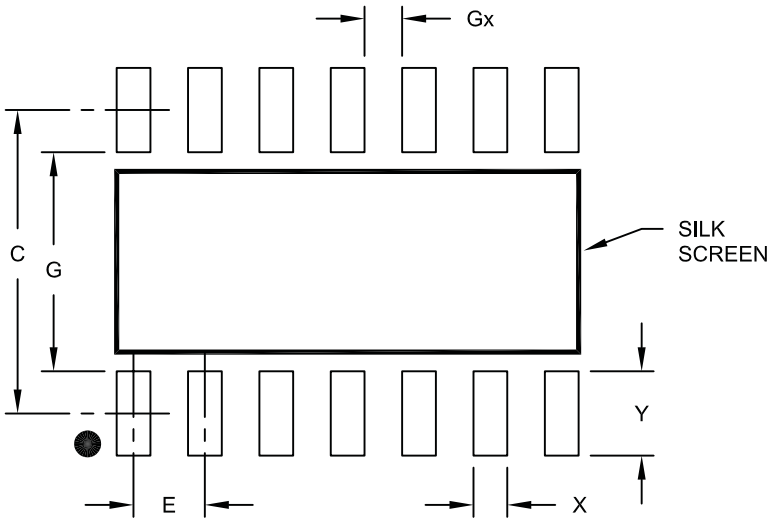
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

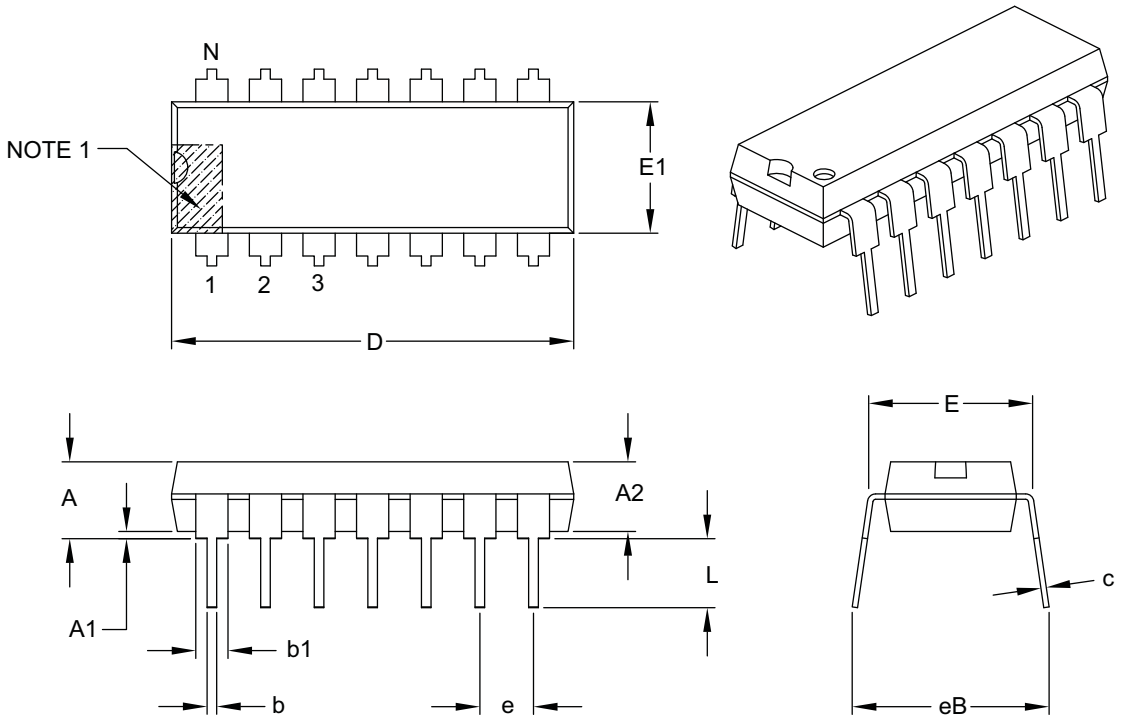
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (October 2017)

The following is the list of modifications:

- Updated **Section 4.8 "Smoke Calibration (TM12, TM13, TM14, TM15)"**.
- Minor editorial corrections.

Revision C (November 2015)

The following is the list of modifications:

- Removed 6V bias voltage for V_{DD} mentioned in Sections 4.1.1, 4.3 and 4.9.
- Minor editorial corrections.

Revision B (November 2014)

The following is the list of modifications:

- Updated the Typical Application drawing.
- Updated the Absolute Maximum Ratings† section.
- Updated Figure 4-1.
- Updated Register 4-1 and Register 4-2.

Revision A (March 2014)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	[T](1)	X
Device	Package	Number of Pins	Tape and Reel	Lead Free

Device:	RE46C200:	Programmable Photoelectric Smoke Detector ASIC	
	RE46C200T:	Programmable Photoelectric Smoke Detector ASIC (Tape and Reel)(1)	
Package:	E	=	Plastic Dual Inline, 300 ml Body, 14-Lead (PDIP)
	S	=	Small Plastic Outline - Narrow, 3.90 mm Body, 14-Lead (SOIC)

Examples:

a) RE46C200E14F: 14LD PDIP package, Lead Free

b) RE46C200S14F: 14LD SOIC package, Lead Free

c) RE46C200S14TF: 14LD SOIC package, Tape and Reel, Lead Free

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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