# UPD1002

## USB Power Delivery Controller

### Highlights

- Integrated USB Power Delivery (PD) PHY
- Support for Power Delivery Message Protocol
- Integrated Voltage and Current ADC Inputs
- Configuration Profile Selection
- On-chip Microcontroller
- SPI Interface
- Commercial and Industrial Grade Temperature Support
- Available in 32-SQFN Package

### Target Applications

- Notebooks
- Ultrabooks
- Desktop PCs
- Docking Stations
- Monitors
- Printers

### Key Benefits

- Integrated USB Power Delivery (PD) PHY
  - Integrated receive termination
  - Requires minimal external components
- Support for Power Delivery Message Protocol
  - Message Generation/Consumption
  - Retry Generation
  - Error Handling
  - State Behavior
- Cable Detect Logic
  - Cable attachment type
- CFG_SEL pins allow selection of multiple profiles
  - Provider
  - Provider/Consumer
  - Consumer
  - Consumer/Provider
- Integrated Voltage (VMON) and Current (IMON) ADC Inputs
- Dead Battery Support
- On-chip Microcontroller
  - Manages I/Os and other signals
  - Implements power delivery policy engine and device policy manager
- Configuration Programming via OTP, or Vendor Defined Messaging
- Supports Low Power Modes
- Serial Peripheral Interface (SPI) Bus
- Internal 3.3 V and 1.8 V Voltage Regulators
- Integrated Oscillator Reduces BOM Costs
- Package
  - 32-pin SQFN (5 x 5 mm)
- Environmental
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C

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# 1.0 INTRODUCTION

## 1.1 General Description

The UPD1002 is a USB Power Delivery (PD) controller designed to adhere to the *USB Power Delivery Specification*. USB Power Delivery allows a host (or device) to provide or consume up to 5 Amps and/or up to 20 Volts of power from a USB PD capable partner device on the other end of the USB cable. USB PD capable standard and custom cables/ connectors are supported, which in most cases are backward compatible with standard USB connections.

The UPD1002 provides a complete USB Power Delivery solution for notebooks/ultrabooks, desktop PCs, monitors, and docking stations, (see Table 1-1, “UPD1002 Package/Pin Configuration Summary,” on page 6 for available configurations and corresponding applications). The functionality of the UPD1002 is selected via two configuration selection pins, **CFG_SEL0** and **CFG_SEL1**, which can be used to select unique PD and system configurations. Designing the UPD1002 into a system can be as simple as selecting a configuration, with no external EEPROM required. Advanced programmability options exist with an external EEPROM installed.

The integrated USB Power Delivery MAC and PHY support provider and consumer operation via the PD communication protocol, as specified in Revision 1.0 (Version 1.2) of the *USB Power Delivery Specification*. Monitoring of VBUS and battery charging is accomplished via the integrated voltage and current ADC inputs. The PHY supports cable ID detection/identification and loopback modes. The PHY includes a 24MHz FSK modulator/demodulator and provides integrated terminations. The USB PD MAC supports both USB PD insertion detection (cold socket) and dead battery cases. The device provides an integrated voltage switch which is used to detect whether the VBUS or VTR (battery) power supply is active, enabling selection of the appropriate power supply at any given time.

The on-chip microcontroller manages the IOs and implements the power delivery local policy engine and device manager. The SPI ROM controller is used by the microcontroller for optional external code execution from ROM. A One Time Programmable (OTP) ROM is integrated in the UPD1002. Integrated 3.3 V and 1.8 V regulators allow device operation from a single power supply. The UPD1002 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the UPD1002 is shown in Figure 1-1.

Power Delivery applications introduce two different types of USB ports. The Upstream Facing Port (UFP) and the Downstream Facing Port (DFP). The UFP and DFP have different usages and attributes due to the nature of their use cases, as detailed below. For a list of available UPD1002 configurations and corresponding target applications, refer to Table 1-1, “UPD1002 Package/Pin Configuration Summary,” on page 6.

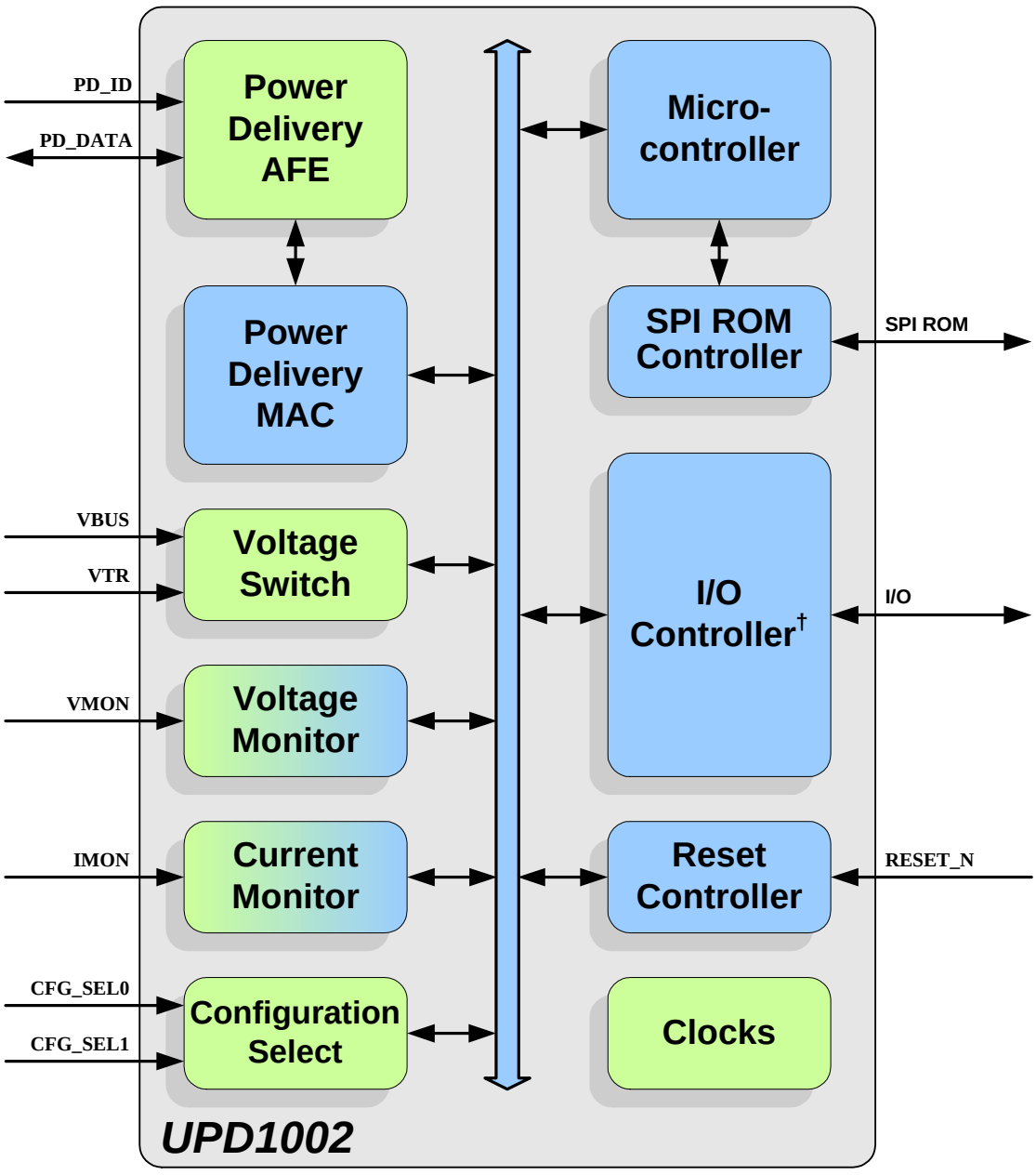
**The Upstream Facing Port (UFP)**

The primary use case of the UFP is to connect to a host computer. In this case, the UFP of the UPD1002 must have a Standard-B (STD-B) USB connector to connect to the host’s Standard-A (STD-A) USB connector. If the host is a notebook/ultrabook, it may request to be charged from the UPD1002 UFP, requiring the system to be wall powered instead of bus-powered. In this case, the UFP must offer a Consumer/Provider role.

**The Downstream Facing Port (DFP)**

The primary use case of the DFP is to connect to other downstream USB devices such as speakers, keyboard, mice, scanners, external hard drives, external optical drives, printers, etcetera. These devices are mainly Consumers in nature in the first phase of adoption. DFPs are Providers by default and have Standard-A USB connectors. Battery Charging 1.2 support can be provided by a parallel USB hub or a Microchip UCS100x or other enhanced port power controller device.

**FIGURE 1-1: INTERNAL BLOCK DIAGRAM**




†*Specific I/O functions are determined by package and **CFG_SEL0/CFG_SEL1** profile selection.*

The UPD1002 is offered in a 32-pin SQFN package. The package provides multiple pin configurations, based upon the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals. Table 1-1 summarizes the available pin combinations and their target applications. Refer to Section 2.0, "Pin Descriptions and Configuration," on page 7 for detailed information on specific pin configurations.

**TABLE 1-1: UPD1002 PACKAGE/PIN CONFIGURATION SUMMARY**

| Package | Pin Config. Name | DFP/ UFP | PD Role | USB Receptacle | Target Applications | Notes |
|---|---|---|---|---|---|---|
| 32-SQFN | 32-P_A | DFP | Provider | Standard-A (STD-A) | • Monitors<br>• Docking stations<br>• Desktop PCs<br>• Printers | See Section 2.1 |
| | 32-CP_B | UFP | Consumer/Provider | Standard-B (STD-B) | • Monitors<br>• Docking stations<br>• Printers | See Section 2.1 |
| | 32-PC_A | DFP | Provider/Consumer | Standard-A (STD-A) | • Notebooks | See Section 2.1<br>No **VSELx_N** |
| | 32-PC_uAB | DFP | Provider/Consumer | Micro-AB (uAB) | • Notebooks<br>• Ultrabooks | See Section 2.1<br>No **VSELx_N** |

## 2.0 PIN DESCRIPTIONS AND CONFIGURATION

The pinouts for the package, along with system-level application diagrams, are detailed in the following section:

- 32-Pin SQFN (32-SQFN)

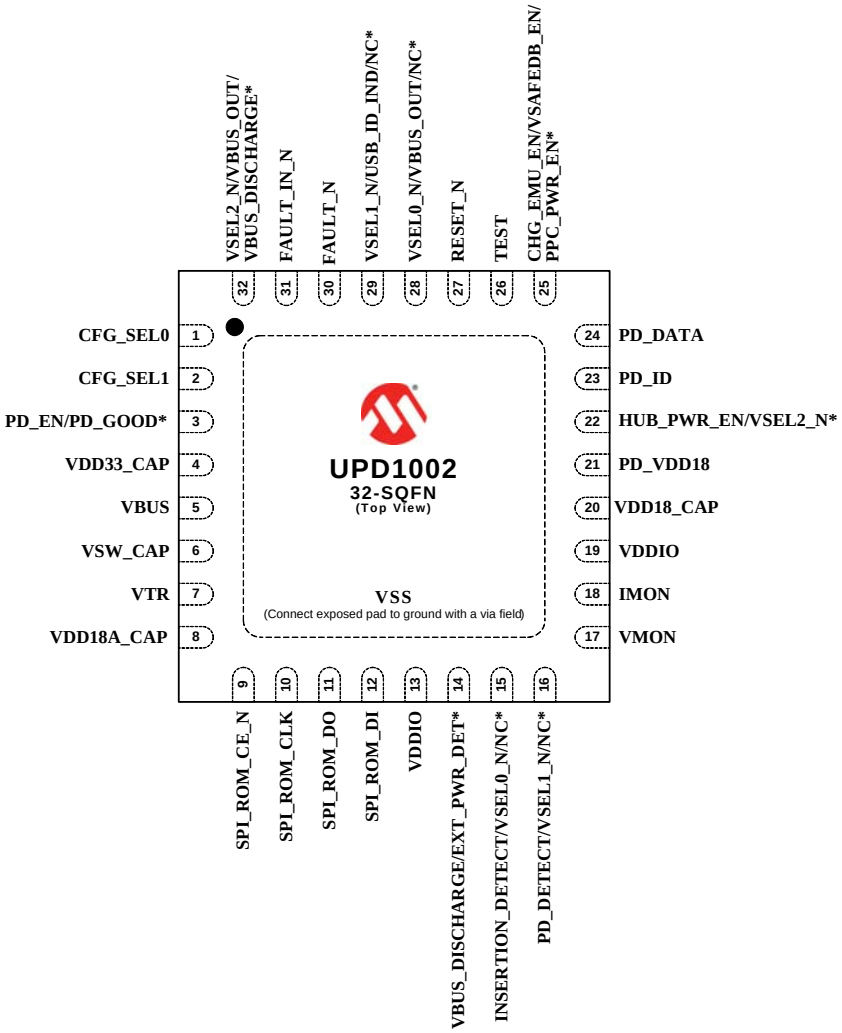
**Note:** For a summary of the available pin combinations and their corresponding target applications, refer to Table 1-1.

Pin descriptions are detailed in Section 2.2, "Pin Descriptions," on page 14. For details on the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals, refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)," on page 24.

### 2.1 32-Pin SQFN (32-SQFN)

#### 2.1.1 32-SQFN PIN DIAGRAM

**FIGURE 2-1: 32-SQFN PIN ASSIGNMENTS (TOP VIEW)**




*The functionality of this pin is dependent on the **CFG_SEL0/CFG_SEL1** profile selection.

**Note:** Exposed pad **(VSS)** on bottom of package must be connected to ground with a via field.

**Note:** When an "**_N**" is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

**Note:** The buffer type for each signal is indicated in the BUFFER TYPE column of Table 2-2, "Pin Descriptions". A description of the buffer types is provided in Section 2.3, "Buffer Types".

### 2.1.2 32-SQFN PIN ASSIGNMENTS

The UPD1002 32-SQFN provides four distinct pin configurations (32-P_A, 32-CP_B, 32-PC_A, and 32-PC_uAB) based upon the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals. These configurations are designed for specific applications, as outlined in Table 1-1, "UPD1002 Package/Pin Configuration Summary," on page 6. The 32-SQFN package pin assignments for each configuration are detailed in Table 2-1. For pin descriptions, refer to Section 2.2, "Pin Descriptions". For example connection diagrams, refer to Section 2.4, "Power Connection Diagram," on page 22. For information on the Configuration Select signals, refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)".

**TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS**

| Pin Number | Configuration 32-P_A Pin Name | Configuration 32-CP_B Pin Name | Configuration 32-PC_A Pin Name | Configuration 32-PC_uAB Pin Name |
|---|---|---|---|---|
| 1 | CFG_SEL0 | | | |
| 2 | CFG_SEL1 | | | |
| 3 | PD_EN | PD_EN | PD_GOOD | PD_GOOD |
| 4 | VDD33_CAP | | | |
| 5 | VBUS | | | |
| 6 | VSW_CAP | | | |
| 7 | VTR | | | |
| 8 | VDD18A_CAP | | | |
| 9 | SPI_ROM_CE_N | | | |
| 10 | SPI_ROM_CLK | | | |
| 11 | SPI_ROM_DO | | | |
| 12 | SPI_ROM_DI | | | |
| 13 | VDDIO | | | |
| 14 | VBUS_DISCHARGE | VBUS_DISCHARGE | EXT_PWR_DET | EXT_PWR_DET |
| 15 | INSERTION_DETECT | VSEL0_N | INSERTION_DETECT | NC |
| 16 | PD_DETECT | VSEL1_N | PD_DETECT | NC |
| 17 | VMON | | | |
| 18 | IMON | | | |
| 19 | VDDIO | | | |
| 20 | VDD18_CAP | | | |
| 21 | PD_VDD18 | | | |
| 22 | HUB_PWR_EN | VSEL2_N | HUB_PWR_EN | HUB_PWR_EN |
| 23 | PD_ID | | | |
| 24 | PD_DATA | | | |
| 25 | CHG_EMU_EN | VSAFEDB_EN | PPC_PWR_EN | PPC_PWR_EN |
| 26 | TEST | | | |
| 27 | RESET_N | | | |

**TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS (CONTINUED)**

| Pin Number | Configuration 32-P_A Pin Name | Configuration 32-CP_B Pin Name | Configuration 32-PC_A Pin Name | Configuration 32-PC_uAB Pin Name |
|---|---|---|---|---|
| 28 | VSEL0_N | NC | NC | VBUS_OUT |
| 29 | VSEL1_N | NC | NC | USB_ID_IND |
| 30 | FAULT_N | | | |
| 31 | FAULT_IN_N | | | |
| 32 | VSEL2_N | VBUS_OUT | VBUS_DISCHARGE | VBUS_DISCHARGE |
| Exposed Pad | VSS | | | |

### 2.1.3 32-SQFN SYSTEM LEVEL DIAGRAMS

Figure 2-2, Figure 2-3, Figure 2-4, and Figure 2-5 provide typical system level diagrams of the UPD1002 for configurations 32-P_A, 32-CP_B, 32-PC_A, and 32-PC_uAB, respectively.

**FIGURE 2-2: CONFIGURATION 32-P_A SYSTEM-LEVEL DIAGRAM**

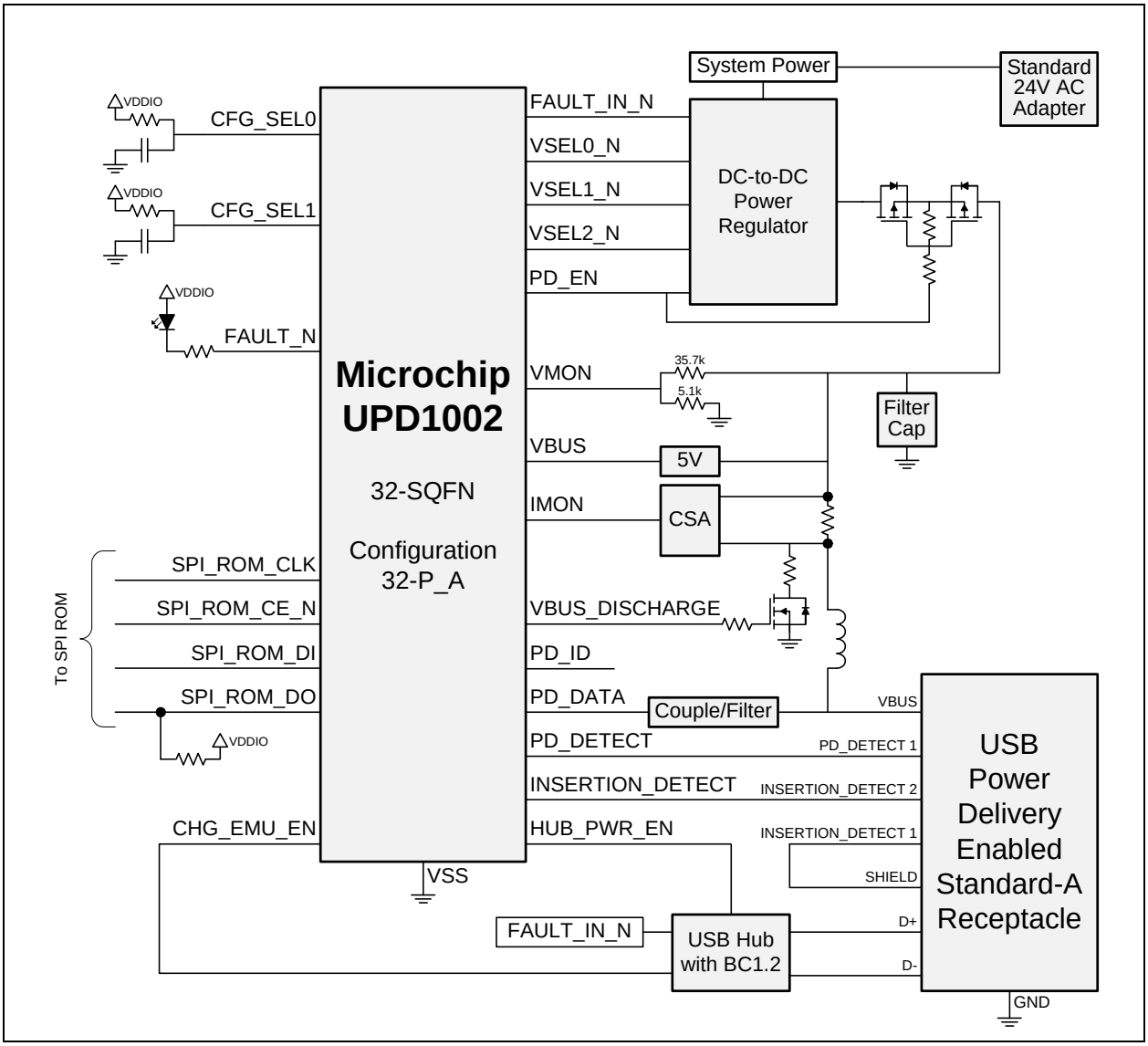


**FIGURE 2-3: CONFIGURATION 32-CP_B SYSTEM-LEVEL DIAGRAM**

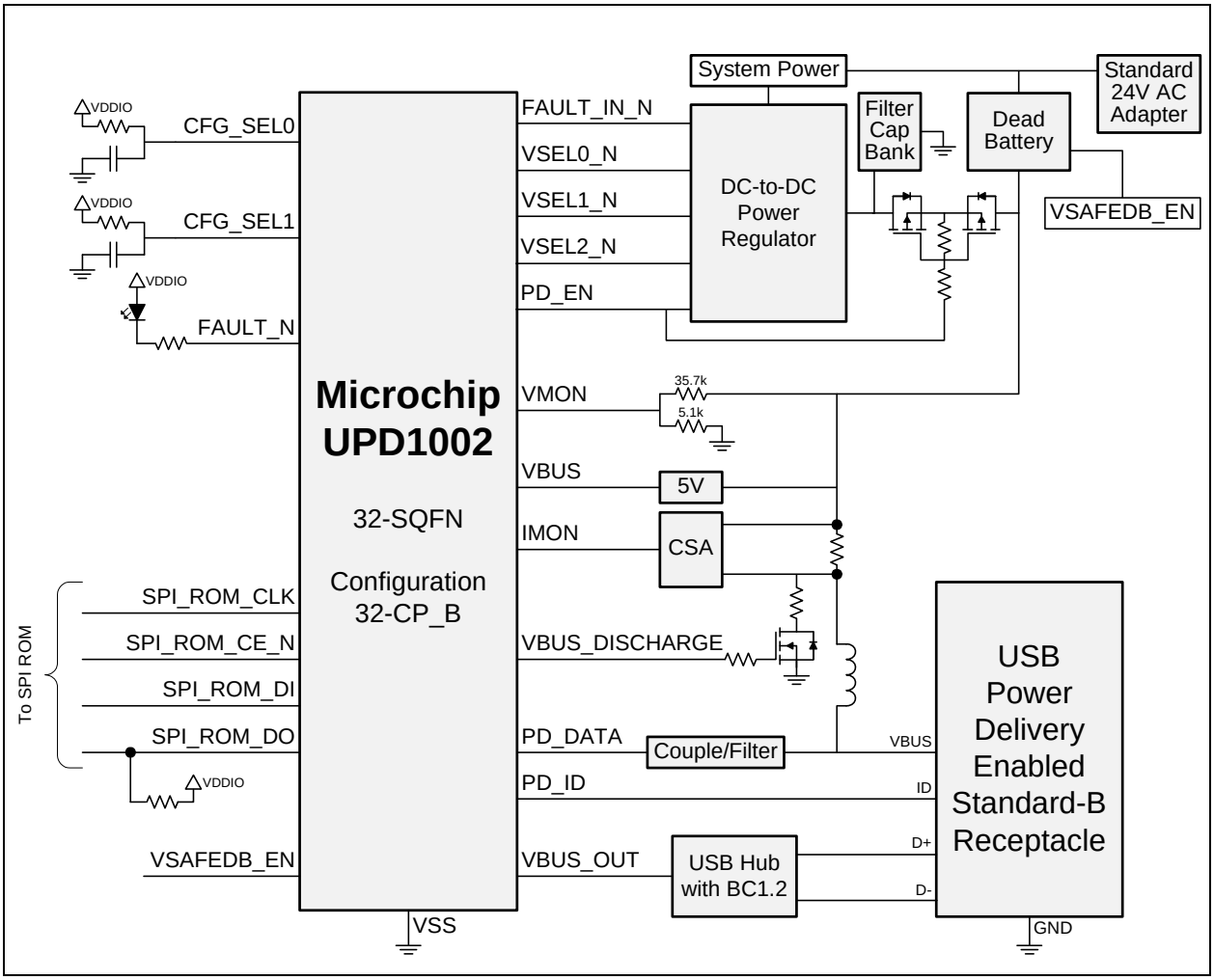


**FIGURE 2-4: CONFIGURATION 32-PC_A SYSTEM-LEVEL DIAGRAM**

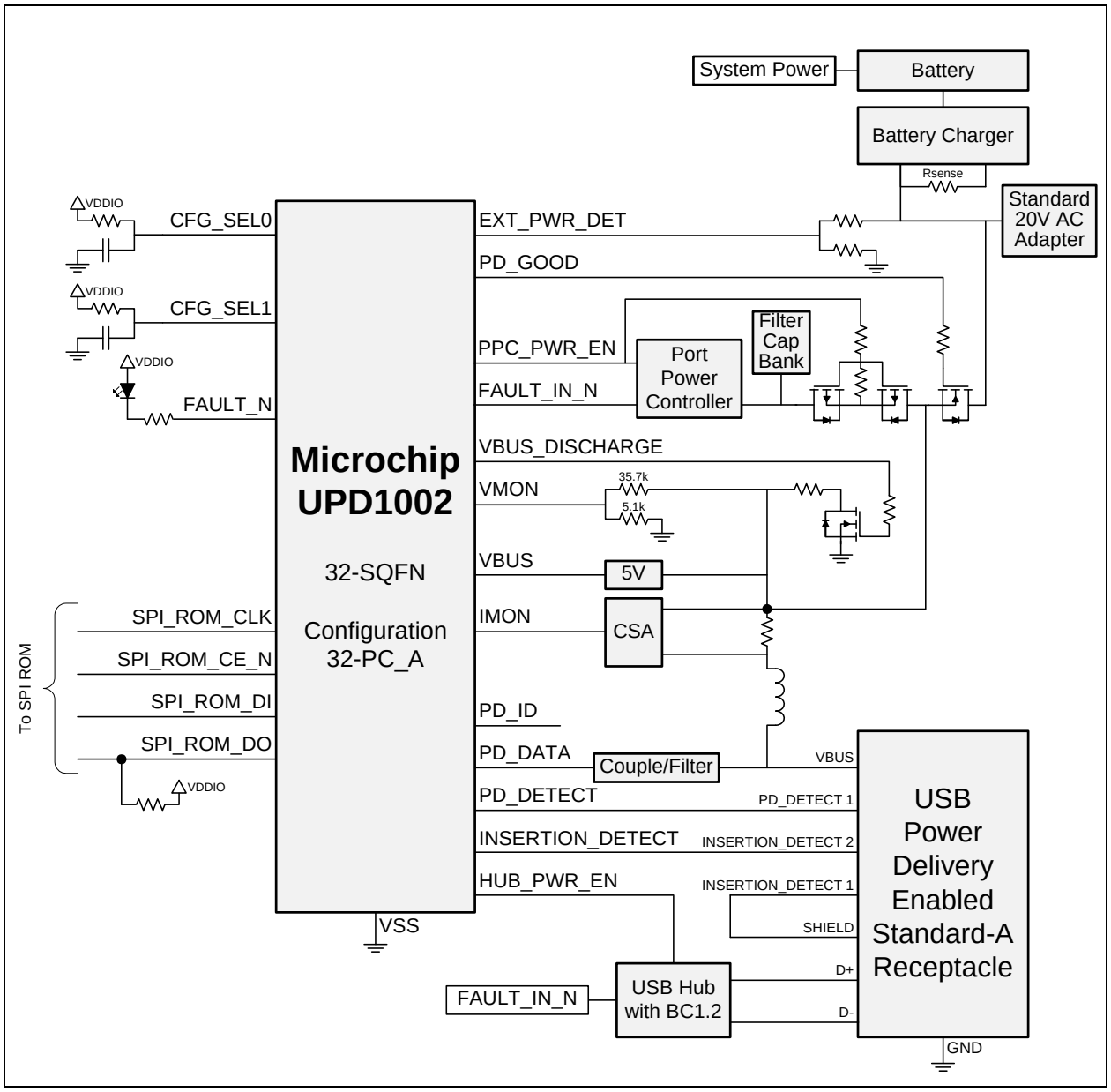
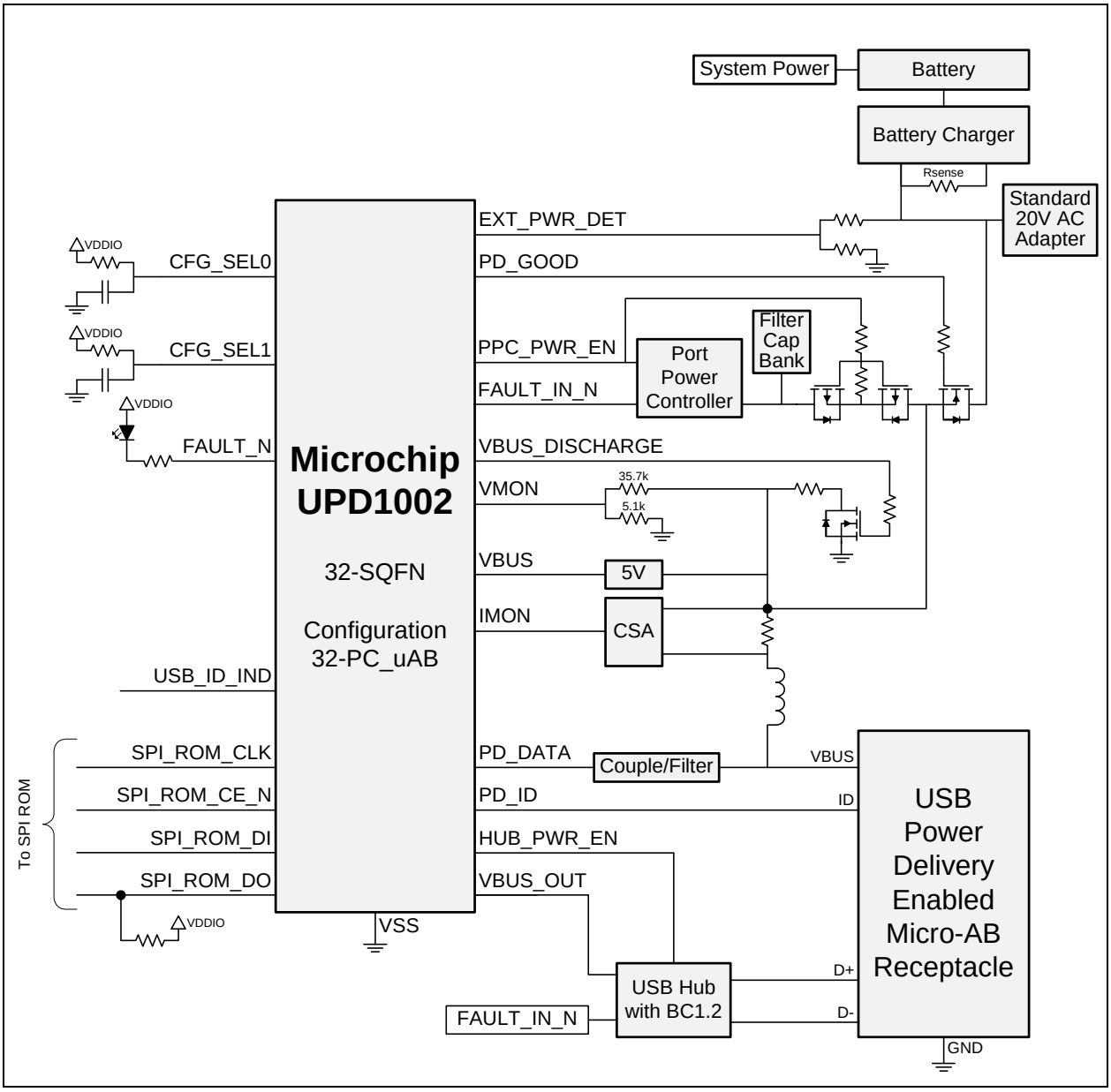


**FIGURE 2-5: CONFIGURATION 32-PC_UAB SYSTEM-LEVEL DIAGRAM**



## 2.2 Pin Descriptions

**TABLE 2-2: PIN DESCRIPTIONS**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| **Power Delivery** | | | |
| Power Delivery Cable ID | **PD_ID** | AIO | USB connector signal used to indicate a high-current power delivery capable cable is inserted. This signal is to be connected to the PD_ID pin located on the USB PD Standard-B receptacle. |
| Power Delivery VBUS Data | **PD_DATA** | AIO | Modulated power delivery VBUS data. Requires in-line isolation filter. Reference schematic available on request. |
| Power Delivery Detect | **PD_DETECT** | IS (PU) | This signal is to be connected to the PD DETECT pins located on the USB PD Standard-A receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) of PD_DETECT qualifies a USB-PD plug detection event. |
| Power Delivery Enable (Active High) | **PD_EN** | O8 | This active high signal is used to drive the enable pin of the DC-to-DC solution direction directly. Alternatively, this signal may be used to drive an N-channel MOSFET into cuttoff and isolate the input power of the DC-to-DC solution.<br>**Note:** This function is only available in specific device configurations. |
| Power Delivery Good | **PD_GOOD** | O8 | This active high signal is asserted whenever a valid USB power delivery contract has been established and the device is operating as a sink in a configuration other than VSafe5V-0A. A valid contract is defined as a PD contract that matches one of the supported PD consumer/provider profiles, as determined by the **CFG_SEL0/CFG_SEL1** configuration. When there is no valid contract established, this signal de-asserts.<br>**Note:** This signal will not be asserted, or become de-asserted, if the VBUS voltage is not within the desired range, as determined by the VMON voltage monitoring (despite a contract being established).<br>**Note:** This function is only available in specific device configurations. |
| **Miscellaneous** | | | |
| VBUS Voltage Monitor | **VMON** | AI | Stepped down voltage representation of the VBUS voltage. This signal must be connected to a voltage divider circuit as specified in Section 2.4, "Power Connection Diagram," on page 22. Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| Charger Current Monitor | **IMON** | AI | Voltage representation of the charger current. This signal should be fed by a current sense amplifier tuned to output 3.0 V when 6.0 A is flowing on VBUS. Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |
| Power Supply Fault Indicator | **FAULT_N** | OD8 | This active low signal can be connected to an external LED or SoC and is used by the device to indicate power supply exceptions/failures as determined by the integrated voltage/current monitors. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 29 for additional information. |
| Fault Input | **FAULT_IN_N** | IS | This active low signal is asserted by the power supplying device (DC to DC controller or port power controller) to notify the device when a system fault condition has occurred. Typically, this signal is used for overcurrent or overvoltage conditions, but it can be used for any system related failure. This signal should be debounced to 1 ms.<br>**Note:** The board design must ensure this signal is in a valid state by the time **PPC_PWR_EN** or **PD_GOOD** asserts. |
| Power Delivery Profile Configuration Selector 0 | **CFG_SEL0** | AIO | This pin is used in conjunction with **CFG_SEL1** to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information. |
| Power Delivery Profile Configuration Selector 1 | **CFG_SEL1** | AIO | This pin is used in conjunction with **CFG_SEL0** to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information. |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| Source Voltage Select 0 | **VSEL0_N** | OD8 | This active low signal is one in a series of output pins (**VSEL0_N**, **VSEL1_N**, and **VSEL2_N**) used to select the correct source voltage from the DC-to-DC solution. Each **VSELx_N** pin is dedicated to one voltage, assigned in order of increasing supported voltage.<br><br>For example, if 5, 12 and 20 V capabilities are supported, the **VSELx_N** selections will be as follows:<br><br>**VSEL0_N** = 5 V<br>**VSEL1_N** = 12 V<br>**VSEL2_N** = 20 V<br><br>In another example, if only 5 and 20 V care supported, the **VSELx_N** selections will be as follows:<br><br>**VSEL0_N** = 5 V<br>**VSEL1_N** = 20 V<br>**VSEL2_N** = RESERVED<br><br>The **VSELx_N** pins are also used to set the overvoltage protection (OVP) voltage on the **VMON** pin. The OVP fault will trigger when the measured voltage on **VMON** is 10% above the selected voltage setting.<br><br>For a mapping of the **VSELx_N** voltage assignments for each **CFG_SEL1/CFG_SEL0** configuration profile, refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)," on page 24.<br><br>**Note:** This function is only available in specific device configurations. |
| Source Voltage Select 1 | **VSEL1_N** | OD8 | This active low signal is one in a series of output pins (**VSEL0_N**, **VSEL1_N**, and **VSEL2_N**) used to select the correct source voltage from the DC-to-DC solution. Each **VSELx_N** pin is dedicated to one voltage, assigned in order of increasing supported voltage.<br><br>Refer to the **VSEL0_N** definition for additional information.<br><br>**Note:** This function is only available in specific device configurations. |
| Source Voltage Select 2 | **VSEL2_N** | OD8 | This active low signal is one in a series of output pins (**VSEL0_N**, **VSEL1_N**, and **VSEL2_N**) used to select the correct source voltage from the DC-to-DC solution. Each **VSELx_N** pin is dedicated to one voltage, assigned in order of increasing supported voltage.<br><br>Refer to the **VSEL0_N** definition for additional information.<br><br>**Note:** This function is only available in specific device configurations. |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| VBUS Discharge | **VBUS_DISCHARGE** | O8 | This active high output is used to drive a power NFET to discharge VBUS during high-to-low voltage transitions in order to achieve vSafe0V. When asserted, the external MOSFET should conduct to GND through a current limiting resistor. This signal de-asserts when the **VMON** signal voltage reaches a preset value (a percentage of the destination voltage). |
| VBUS Out | **VBUS_OUT** | O8 | This active high output is used on an Upstream Facing Port (UFP) to tell the hub to stay connected. This signal will remain asserted at all times that a valid VBUS level is present (VBUS minimum of 4.5 V to PD VBUS maximum 20 V+10%) on the UFP, as well as during any voltage transitions or role swaps where the voltage may drop below 4.5V.<br>**Note:** Per the OTG specification, data connectivity roles can be swapped and a micro-AB connector with a micro-A plug inserted can operate as an “upstream” port (as a device). Therefore, **VBUS_OUT** assertion behavior as per above is not only valid with a micro-B cable, but also a micro-A cable so that the USB data link is not lost during PD swaps.<br>**Note:** This function is only available in specific device configurations. |
| USB ID Indicator | **USB_ID_IND** | O8 | This signal is used in micro-AB pinouts to indicate to the OTG host whether a micro-A plug (Legacy, Low Power or PD) is present. If a micro-A plug is present, this pin is low. Otherwise it is high. |
| Emulation Enable | **CHG_EMU_EN** | O8 | This active high output signal can be used to drive the Emulation Enable pin of a Microchip UCS1001 or similar device that supports BC 1.2. The device will assert this signal whenever operating at VSafe5V without a PD contract. Whenever a PD contract is established (even at 5 V), this signal is de-asserted.<br>**Note:** This function is only available in specific device configurations. |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| Insertion Detect | **INSERTION_DETECT** | IS (PU) | This active low input signal should be connected to the Insertion Detect pin on the USB Standard-A (STD-A) receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) qualifies a STD-A plug insertion event and triggers transition out of the “Startup” state of the Source Policy engine.<br>The device firmware implements cold socket detection using the **INSERTION_DETECT** signal. Even when operating as a provider, if the signal is high, the device will not output voltage on VBUS. VSafe5V will only be output upon assertion of this signal (low).<br>**Note:** Cold socket (insertion detect) is an optional feature in the USB PD specification. If this feature is not being used in a design, the **INSERTION_DETECT** signal must be grounded.<br>**Note:** This function is only available in specific device configurations. |
| Dead Battery Enable | **VSAFEDB_EN** | O8 | This active high output signal is used to enable the dead battery supply on a USB Standard-B (STD-B) receptacle (consumer/provider) AC adapter. When no voltage has been detected on VBUS, this signal is asserted every 10 s to back power an attached provider/consumer and determine whether the attached device has specified to be powered per the dead battery mechanisms specified in the PD specification.<br>**Note:** This function is only available in specific device configurations. |
| External Power Source Detect | **EXT_PWR_DET** | IS | This active high signal is used to indicate an external power source is installed. This input can be utilized as a standard digital input, or a resistive voltage divider can be used to determine if the wall power AC adapter or charger is plugged into the platform (i.e., a qualifying “Externally Powered” status has occurred, according to the USB Power Delivery Specification). In a typical application, this signal level will be set by a resistor divider of the DC barrel voltage to satisfy the device logic levels and level tolerance.<br><br>When this signal is high, the “externally powered” bit of the VSafe5V Fixed Supply PDO for a provider will be set.<br><br>This signal will also help determine the preferences on role swaps. Refer to Section 3.3.4, "USB Power Delivery Role Selection," on page 26 for additional information.<br>**Note:** This function is only available in specific device configurations. |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| Hub Power Enable | **HUB_PWR_EN** | IS | This active high signal is driven by either the PCH of a notebook or a downstream facing port (DFP) on a USB hub. The hub or USB host may request the port to be turned off by de-asserting this signal. Upon de-assertion, if the device is NOT operating as a sink under a PD contract, the device will de-assert the **PD_EN** signal to turn off VBUS to the port, which will remain off until **HUB_PWR_EN** asserts again.<br>**Note:** In the case that the port supports insertion detect or has a micro-AB receptacle (which must support plug detection), the **HUB_PWR_EN** signal is ignored unless there is a STD-A or micro-A plug inserted.<br>**Note:** This function is only available in specific device configurations. |
| Port Power Controller Enable | **PPC_PWR_EN** | O8 | This active high signal is used to enable an attached port power controller. It should only be used in cases in which the only source capability offered is 5 V.<br>**Note:** In cases where the port power controller supports BC or other charging profiles, this single signal will be enabling both power sourcing as well as enabling the handshake emulation. BC handshaking will occur before PD negotiation and if in a headless/DCP charging mode, the handshake will persist even after a PD negotiation was completed successfully.<br>**Note:** This function is only available in specific device configurations. |
| System Reset | **RESET_N** | IS (PU) | System reset. This signal is active low. |
| Test | **TEST** | IS | Test signal. This signal is used for internal purposes only and must be connected to ground through a 1 K resistor for normal operation. |
| No Connect | **NC** | - | No connect. For proper operation, this signal must not be connected. |
| **SPI ROM Interface** | | | |
| SPI ROM Clock | **SPI_ROM_CLK** | O8 | SPI clock output to the serial ROM |
| SPI ROM Chip Enable | **SPI_ROM_CE_N** | O8 | This is the active low SPI ROM chip enable output. If the SPI ROM interface is enabled, this signal should be pulled up to the SPI ROM Vcc rail. |
| SPI ROM Data In | **SPI_ROM_DI** | IS | SPI ROM data in |

**TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)**

| Name | Symbol | Buffer Type | Description |
|---|---|---|---|
| SPI ROM Data Out | **SPI_ROM_DO** | O8 (PD) | SPI ROM data out<br>**Note:** This signal must be pulled-up to VDDIO with an external 10 kΩ resistor for proper operation. |
| **Power/Ground** | | | |
| VTR Supply Input | **VTR** | P | +3.3 to +5.0 V main power supply input. This signal must be connected to a 2.2 µF capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +3.3 to +5.0 V Variable Voltage I/O Power | **VDDIO** | P | +3.3 V to +5.0 V variable I/O power supply input. Refer to Figure 2-6 for additional power connection information.<br>**Note:** When using internal +3.3 V regulator, these pins must be externally connected to **VDD33_CAP**. |
| +5.0 V VBUS Input | **VBUS** | P | +5.0 V VBUS input. This signal provides power in the dead battery case. This signal must be connected to a 2.2 µF capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +1.8V Power Delivery | **PD_VDD18** | P | +1.8 V power for Power Delivery PHY. Refer to Figure 2-6 for additional power connection information.<br>**Note:** This pin must be connected to **VDD18_CAP** pin externally when using the internal VDD18 regulator. |
| +1.8 V Power Capacitance | **VDD18_CAP** | P | This pin is used to provide capacitance for the integrated +1.8 V regulator and must be connected to a 1 µF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +1.8 V Analog Power Capacitance | **VDD18A_CAP** | P | This pin is used to provide capacitance for the integrated +1.8 V analog regulator and must be connected to a 1 µF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| +3.3 V Power Capacitance | **VDD33_CAP** | P | +3.3 V regulator output. This pin must be connected to a 1 µF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| Integrated Power Switch Capacitance | **VSW_CAP** | P | This pin is used to provide capacitance for the integrated power switch and must be connected to a 1 µF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-6 for additional power connection information. |
| Ground | **VSS** | P | Common ground. This exposed pad must be connected to the ground plane with a via array. |

## 2.3 Buffer Types

**TABLE 2-3: BUFFER TYPES**

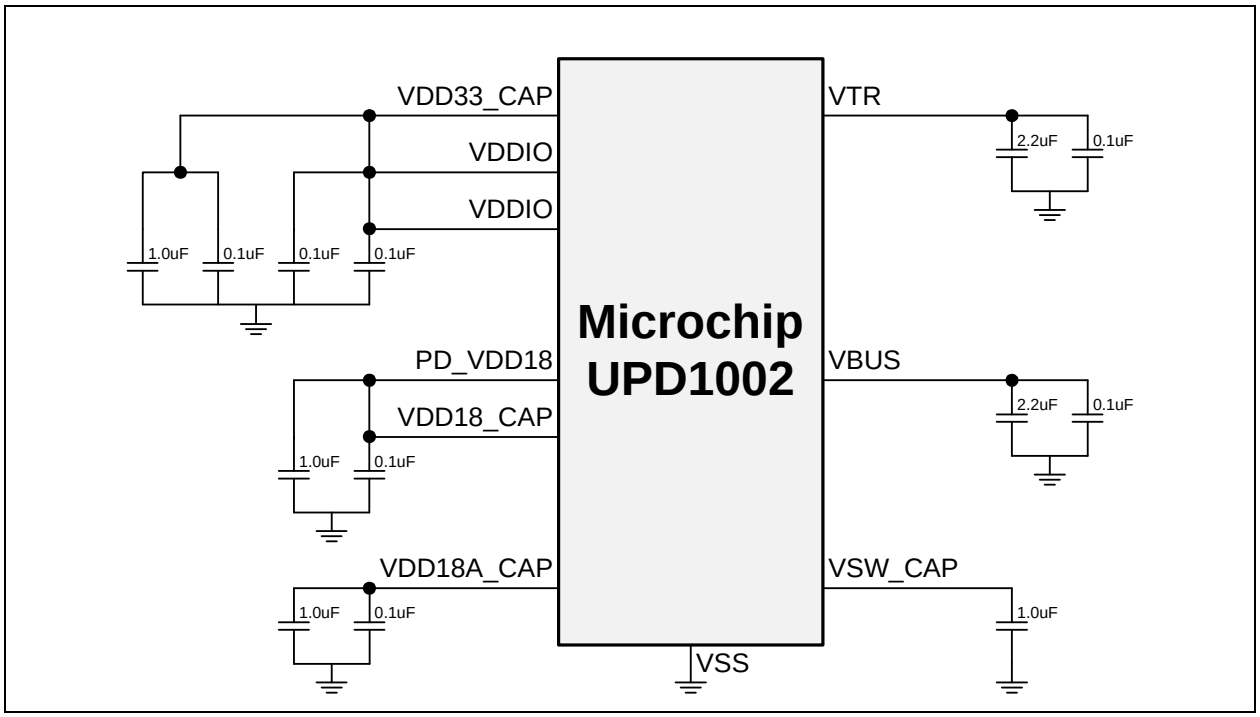
| Buffer Type | Description |
|---|---|
| IS | Schmitt-triggered input |
| O8 | Output with 8 mA sink and 8 mA source |
| OD8 | Open-drain output with 8 mA sink |
| PU | 50 µA (typical) internal pull-up. Unless otherwise noted in the signal description, internal pull-ups are always enabled.<br>**Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 µA (typical) internal pull-down. Unless otherwise noted in the signal description, internal pull-downs are always enabled.<br>**Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AI | Analog input |
| AIO | Analog bi-directional |
| P | Power pin |

**Note:** All signals are 5 V tolerant.

## 2.4 Power Connection Diagram

Figure 2-6 details the various power connection requirements.

**FIGURE 2-6: POWER CONNECTION DIAGRAM**



# 3.0 FUNCTIONAL DESCRIPTIONS

This chapter provides functional descriptions for the various device sub-systems:

- Resets
- Power Management
- Configuration Selection (CFG_SEL0/CFG_SEL1)
- Voltage/Current Monitors (VMON/IMON)
- SPI ROM Controller

## 3.1 Resets

The device includes the following reset controls:

- Power-On Reset (POR)
- External Chip Reset (**RESET_N**)

A system reset event via the external **RESET_N** pin or POR causes the following:

- All registers are set to their default values
- Pins are placed into their default state

The rising and falling Power-On Reset thresholds for each power supply are detailed in Table 3-1.

**TABLE 3-1: POR THRESHOLDS**

| POR | Rising Threshold | Falling Threshold |
|---|---|---|
| **VDDIO** Supply | 2.7 V | 2.35 V |
| **VTR** Supply | 2.85 V | 2.7 V |

After power up, the POR initially de-asserts after the Rising Threshold is passed. In the event that the supply drops below the Falling Threshold, the POR will assert. The POR stays asserted until the Rising Threshold is once again crossed.

## 3.2 Power Management

The device will enter low power modes based on the state of the connection to the power delivery port partner. The low power connection states are defined for the device operating as a Provider (Provider/Consumer) or a Consumer (Consumer/Provider).

The device provides the following power states:

- Provider: Wait Insert State
- Consumer: Sink Discovery State

### 3.2.1 PROVIDER (OR PROVIDER/CONSUMER) POWER STATE

The device Provider configuration will enter a low power mode when it is not connected to a port partner and when a Standard-A plug is not inserted in the receptacle.

#### 3.2.1.1 Wait Insert State

In the Wait Insert State, the device utilizes the insertion detect feature to enter a standby mode when waiting for a Standard-A plug to be inserted in the receptacle. On insertion of a Standard-A plug, the device will exit from the standby mode, initiate operation by enabling the supply output to 5Vsafe, and initiate the discovery of a port partner.

### 3.2.2 CONSUMER (OR CONSUMER/PROVIDER) POWER STATE

The device Consumer configuration enters a standby mode when it is not connected to a provider.

#### 3.2.2.1 Sink Discovery State

In the Sink Discovery State, the device waits for the presence of VBUS to indicate a connection to provider. The device enters a standby state when waiting for the presence of VBUS. At the presence of VBUS, the Consumer exits the standby state and resumes full operation to establish a negotiated power contract with the Provider.

## 3.3 Configuration Selection (CFG_SEL0/CFG_SEL1)

The UPD1002 provides a resistor/capacitor identification detection interface which is utilized to set various device configuration parameters via the Configuration Select pins:

- **CFG_SEL0**
- **CFG_SEL1**

Each Configuration Select pin can discriminate a number of quantized RC constants. The judicious selection of RC values provides a low cost means for system element configuration identification. The Configuration Select pins measure the charge/discharge time for the RC circuit connected to it (shown in Figure 3-1), providing the ability to differentiate 16 unique “bins” for each Configuration Select pin. The resistor and capacitor values for each Configuration Select bin are defined in Table 3-2.

**FIGURE 3-1: CFG_SEL0/CFG_SEL1 RESISTOR-CAPACITOR CIRCUIT CONNECTIONS**

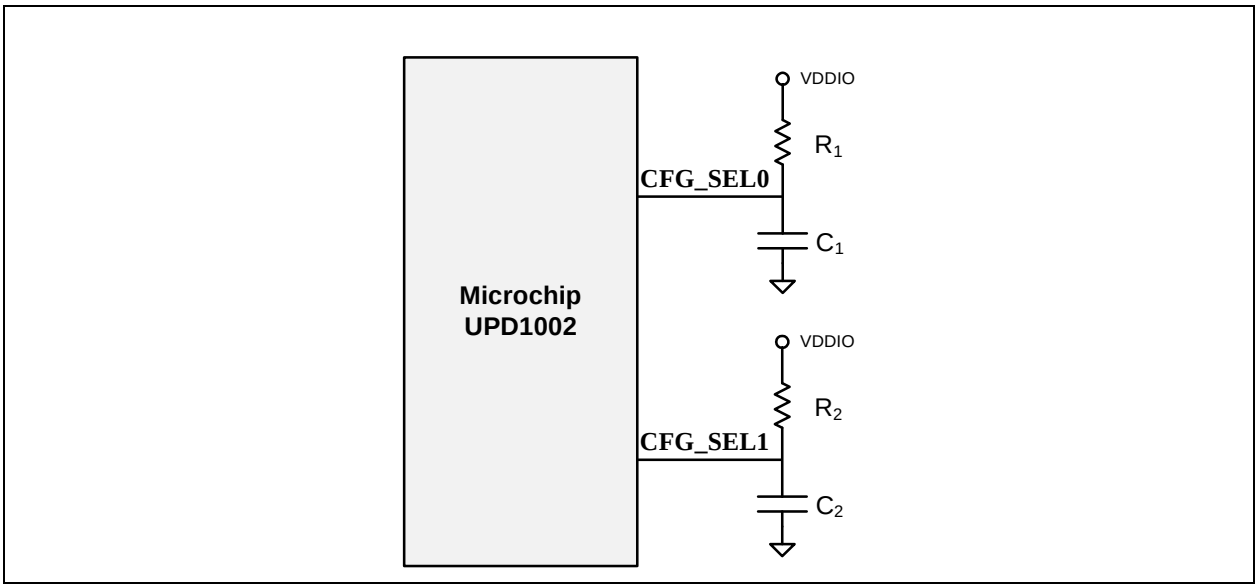



**TABLE 3-2: CFG_SELX PIN RESISTOR-CAPACITOR BIN ALLOCATION**

| Bin | $R_X$ (+/-1%) | $C_X$ (+/-5%) |
|---|---|---|
| 1 | 2.70 kΩ | None |
| 2 | 2.70 kΩ | 470 pF |
| 3 | 4.87 kΩ | 470 pF |
| 4 | 8.66 kΩ | 470 pF |
| 5 | 15.40 kΩ | 470 pF |
| 6 | 2.70 kΩ | 4.7 nF |
| 7 | 4.87 kΩ | 4.7 nF |
| 8 | 8.66 kΩ | 4.7 nF |
| 9 | 15.40 kΩ | 4.7 nF |
| 10 | 2.70 kΩ | 47.0 nF |
| 11 | 4.87 kΩ | 47.0 nF |
| 12 | 8.66 kΩ | 47.0 nF |
| 13 | 15.40 kΩ | 47.0 nF |
| 14 | 2.70 kΩ | 470 nF |
| 15 | 4.87 kΩ | 470 nF |
| 16 | 8.66 kΩ | 470 nF |

**Note:** **CFG_SEL0** and **CFG_SEL1** bin definitions are identical.

By selecting specific bins on both the **CFG_SEL0** and **CFG_SEL1** pins, predefined configurations, unique to each package, may be selected. These assignments configure multiple parameters of the device, including the following:

- Pin Configuration
- Receptacle Type
- USB Power Delivery Role Selection

A list of the configuration assignments, along with the corresponding **CFG_SEL0** and **CFG_SEL1** bin settings, are detailed in the following section:

- Section 3.3.1, "32-SQFN CFG_SELx Configuration Assignments," on page 25

For details on each configurable parameter, refer to the following sub-sections.

**Note:** Only the bin combinations defined in the following tables are valid. All other bin combinations are reserved and must not be used.

**Note:** All configurations can run from either internal ROM or external SPI ROM, providing an easy design transition path from the UPD1000 with external SPI to the UPD1002 with internal ROM.

### 3.3.1 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS

Table 3-3 details the various 32-SQFN **CFG_SELx** configuration assignments.

**TABLE 3-3: 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS**

| Config. # | Application | 32-SQFN Pin Config. | USB Receptacle Type | PD Consumer Abilities | PD Provider Abilities | VSEL0_N | VSEL1_N | VSEL2_N | CFG_SEL1 Bin | CFG_SEL0 Bin |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | DFP Provider | 32-P-A | STD-A | None | Profile 1 | 5V | - | - | 3 | 1 |
| 2 | | | | | Profile 2 | 5V | 12V | - | 3 | 2 |
| 3 | | | | | Profile 3 | 5V | 12V | - | 3 | 3 |
| 4 | | | | | Profile 4 | 5V | 12V | 20V | 3 | 4 |
| 5 | | | | | Profile 5 | 5V | 12V | 20V | 3 | 5 |
| 6 | UFP Consumer/Provider | 32-CP_B | STD-B | VSafe5V-NC | 12V@1.5A | 5V | 12V | - | 3 | 6 |
| 7 | | | | | 12V@3A | 5V | 12V | - | 3 | 7 |
| 8 | | | | | 12V@5A | 5V | 12V | - | 3 | 8 |
| 9 | | | | | 20V@3A | 5V | 20V | - | 4 | 1 |
| 10 | | | | | 20V@5A | 5V | 20V | - | 4 | 2 |
| 11 | | | | | Profile 4 | 5V | 12V | 20V | 4 | 3 |
| 12 | | | | | Profile 4, PP-200 | 5V | 12V | 20V | 4 | 4 |
| 13 | | | | | Profile 5 | 5V | 12V | 20V | 4 | 5 |
| 14 | | | | | Profile 5, PP-200 | 5V | 12V | 20V | 4 | 6 |
| 15 | Provider/Consumer | 32-PC_A | STD-A | 12V@1.5A | VSafe5V-L | N/A | N/A | N/A | 1 | 1 |
| 16 | | | | 12V@3A | VSafe5V-L | N/A | N/A | N/A | 1 | 2 |
| 17 | | | | 12V@3A | Profile 1 | N/A | N/A | N/A | 1 | 3 |
| 18 | | | | 12V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 4 |
| 19 | | | | 12V@5A | Profile 1 | N/A | N/A | N/A | 1 | 5 |
| 20 | | | | 12V@5A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 6 |
| 21 | | | | 20V@3A | Profile 1 | N/A | N/A | N/A | 1 | 7 |
| 22 | | | | 20V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 1 | 8 |
| 23 | | | | 20V@5A | Profile 1 | N/A | N/A | N/A | 2 | 1 |
| 24 | | | | 20V@5A | Profile 1, PP-200 | N/A | N/A | N/A | 2 | 2 |

**TABLE 3-3: 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS (CONTINUED)**

| Config. # | Application | 32-SQFN Pin Config. | USB Receptacle Type | PD Consumer Abilities | PD Provider Abilities | VSEL0_N | VSEL1_N | VSEL2_N | CFG_SEL1 Bin | CFG_SEL0 Bin |
|---|---|---|---|---|---|---|---|---|---|---|
| 25 | Provider/Consumer | 32-PC_uAB | uAB | 12V@1.5A | VSafe5V-L | N/A | N/A | N/A | 2 | 3 |
| 26 | | | | 12V@3A | VSafe5V-L | N/A | N/A | N/A | 2 | 4 |
| 27 | | | | 12V@3A | Profile 1 | N/A | N/A | N/A | 2 | 5 |
| 28 | | | | 12V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 2 | 6 |
| 29 | | | | 20V@3A | Profile 1 | N/A | N/A | N/A | 2 | 7 |
| 30 | | | | 20V@3A | Profile 1, PP-200 | N/A | N/A | N/A | 2 | 8 |

### 3.3.2 PIN CONFIGURATION

The UPD1002 32-SQFN package provides selectable pin configurations via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in Table 3-3, "32-SQFN CFG_SELx Configuration Assignments". Table 1-1, "UPD1002 Package/Pin Configuration Summary" provides a summary of the available pin configurations . Refer to Section 2.1, "32-Pin SQFN (32-SQFN)" for details on the package pin definitions.

### 3.3.3 RECEPTACLE TYPE

The USB receptacle type is configurable between Standard-A, Standard-B, and Micro-AB types via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)". Each of these receptacle type settings is detailed below.

#### 3.3.3.1 Standard-A (STD-A)

The Standard-A setting informs the device that the designer is utilizing a Standard-A USB PD receptacle.

#### 3.3.3.2 Standard-B (STD-B)

The Standard-B setting informs the device that the designer is utilizing a Standard-B USB PD receptacle.

#### 3.3.3.3 Micro-AB (uAB)

The Micro-AB setting informs the device that the designer is utilizing a Micro-AB USB PD receptacle.

### 3.3.4 USB POWER DELIVERY ROLE SELECTION

The Power Delivery Provider and Consumer capabilities are detailed in the following sub-sections. Depending on the pin configuration selected, the device may support and swap Consumer and Provider roles. The swapping rules for each configuration are defined as follows:

**Note:** For summary of all device pinouts and their associated Power Delivery capabilities, refer to Table 1-1, "UPD1002 Package/Pin Configuration Summary".

**Downstream Facing Port (DFP) Provider Configurations (32-P_A)**

DFP Provider (STD-A receptacle) configurations only support the Provider role and therefore do not support role swap.

**Upstream Facing Port (UFP) Consumer/Provider Configurations (32-CP_B)**

UFP Consumer/Provider (STD-B receptacle) configurations start operation in their default role of consumers and support role swapping. Swapping rules for UFP Consumer/Provider configurations are defined as follows:

- When operating as a Consumer:
  - Upon starting up, the UFP automatically initiates a swap request to its partner to become a Provider. If the partner rejects the request, the UFP will remain in its Consumer role until the partner requests a swap.
  - If the device receives a swap request from its partner to become a Consumer, it automatically accepts it.

- When operating as a Provider:
  - The UFP will never initiate a swap request to its partner to become a Consumer.
  - If the device receives a swap request from its partner to become a Consumer, it automatically accepts it and will remain in the Consumer role (until the partner requests another swap back to provider, or there is a hard reset or other exception condition that causes the protocol to be reinitiated from startup). The behavior accounts for a partner that may have its own other external power which it decided to use instead of the UFP's.

**Provider/Consumer (STD-A) Configurations (32-PC_A)**

Swapping rules for Provider/Consumer (STD-A receptacle) configurations are defined as follows:

- When operating as a Provider:
  - If externally powered:
    - Do not initiate swap
    - Do not accept swap
  - If not externally powered:
    - Initiate swap
    - Accept swap
- When operating as a Consumer:
  - If externally powered:
    - Initiate swap
    - Accept swap
  - If not externally powered:
    - Do not initiate swap
    - Do not accept swap

**Provider/Consumer (Micro-AB) Configurations (32-PC_uAB)**

Swapping rules for Provider/Consumer (Micro-AB receptacle) configurations are dependent on the connected plug type.

When a Micro-A plug is not connected (ID pin to GND >= 1MΩ, no plug connected, or Micro-B plug connected), the device operates as a Consumer only and does not support role swaps.

When a Micro-A plug is connected (ID pin to GND < 1MΩ), the device operates as a Provider/Consumer with the following rules:

- When operating as a Provider:
  - If externally powered:
    - Do not initiate swap
    - Do not accept swap
  - If not externally powered:
    - Initiate swap
    - Accept swap
- When operating as a Consumer:
  - If externally powered:
    - Initiate swap
    - Accept swap
  - If not externally powered:
    - Do not initiate swap
    - Do not accept swap

#### 3.3.4.1 Power Delivery Provider Capabilities

The USB PD Provider capabilities may be selected via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)". Each of the PD Provider capabilities are detailed below. When capabilities are combined, it is possible that a device can support two or more currents for the same voltage. In this case, the device will only advertise one voltage with the highest current.

For example, a device that specifies support for “Profile 2 + 5V@3A” must support 5V@2A, 12V@1.5A and 5V@ 3A. In this case, the device will advertise only two Power Data Objects (PDO): 5V@3A and 12V@1.5A. The device will not explicitly advertise 5V@2A. However, a consumer that requires 5V@2A will request the 5V@ 3A PDO but only consume 2A.

**VSafe5V-L (5V@1A)**

The Provider Capability Profile for VSafe5V Legacy (5V@1A) indicates that the UPD1002 supports providing 5 V at 1 A. This is typically used in dual-role ports that offer no real capability at 5 V (e.g., a Standard-B Consumer-Provider Monitor UFP that only supports 20 V), but need to abide by the *USB Power Delivery Specification* requirement that at least one VSafe5V PDO be offered. Therefore, the capabilities of a legacy USB port (max 900 mA for USB 3.0) are included.

**Profile 1**

The Provider Capability Profile 1 indicates that the UPD1002 supports providing the voltages and currents needed to satisfy the USB PD profile 1, as defined by the *USB Power Delivery Specification* (5V@2A).

**Profile 2**

The Provider Capability Profile 2 indicates that the UPD1002 supports providing the voltages and currents needed to satisfy the USB PD profile 2, as defined by the *USB Power Delivery Specification* (5V@2A and 12V@1.5A).

**Profile 3**

The Provider Capability Profile 3 indicates that the UPD1002 supports providing the voltages and currents needed to satisfy the USB PD profile 3, as defined by the *USB Power Delivery Specification* (5V@2A and 12V@3A).

**Profile 4**

The Provider Capability Profile 4 indicates that the UPD1002 supports providing the voltages and currents needed to satisfy the USB PD profile 4, as defined by the *USB Power Delivery Specification* (5V@2A, 12V@3A, and 20V@3A).

**Profile 5**

The Provider Capability Profile 5 indicates that the UPD1002 supports providing the voltages and currents needed to satisfy the USB PD profile 5, as defined by the *USB Power Delivery Specification* (5V@2A, 12V@5A, and 20V@5A).

**12V@1.5A**

The Provider Capability 12V@1.5A indicates that the UPD1002 supports providing 12 V at 1.5 A. This option can be combined with other provider capability options.

**12V@3A**

The Provider Capability 12V@3A indicates that the UPD1002 supports providing 12 V at 3 A. This option can be combined with other provider capability options.

**12V@5A**

The Provider Capability 12V@5A indicates that the UPD1002 supports providing 12 V at 5 A. This option can be combined with other provider capability options.

**20V@3A**

The Provider Capability 20V@3A indicates that the UPD1002 supports providing 20 V at 3 A. This option can be combined with other provider capability options.

**20V@5A**

The Provider Capability 20V@5A indicates that the UPD1002 supports providing 20 V at 5 A. This option can be combined with other provider capability options.

**Peak Power-Capable Setting 0b11 - 200% (PP-200)**

The Peak Power-Capable 200% indicates that the UPD1002 supports providing 200% of the current limit for a 1 ms time duration at 5% duty cycle. This will add the correct 0b11 bits to the PDO.

#### 3.3.4.2 PD Consumer Capabilities

The USB PD Consumer capabilities may be selected via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)". Each of the PD Consumer capabilities are detailed below.

**VSafe5V-NC (5V@0A)**

The Consumer Capability Profile for VSafe5V Non-Consuming indicates to the UPD1002 that this solution must have only 5 V input sources and must not consume. This is typically used in dual-role ports that offer no capability in their default role (e.g., a Standard-B Consumer-Provider hub UFP). Additionally, even if not explicitly listed, this capability is supported by all consumers that support no other 5V capability (per the *Power Delivery Specification*).

**12V@1.5A**

The Consumer Capability 12V@1.5A indicates that the UPD1002 must have only 12 V input sources and must have at least 1.5 A of input current for full-featured operation.

**12V@3A**

The Consumer Capability 12V@3A indicates that the UPD1002 must have only 12 V input sources and must have at least 3 A of input current for full-featured operation.

**12V@5A**

The Consumer Capability 12V@5A indicates that the UPD1002 must have only 12 V input sources and must have at least 5 A of input current for full-featured operation.

**20V@3A**

The Consumer Capability 20V@3A indicates that the UPD1002 must have only 20 V input sources and must have at least 3 A of input current for full-featured operation.

**20V@5A**

The Consumer Capability 20V@5A indicates that the UPD1002 must have only 20 V input sources and must have at least 5 A of input current for full-featured operation.

## 3.4 Voltage/Current Monitors (VMON/IMON)

### 3.4.1 VMON

The integrated voltage monitor utilizes the **VMON** pin to read a stepped down voltage representation of the VBUS voltage. This pin must be connected to a voltage divider circuit as specified in Section 2.4, "Power Connection Diagram," on page 22. The device monitors the VBUS voltage as a provider to manage the behavior of the power supply, detecting power supply transitions and over/under-voltage conditions.

The device also monitors the VBUS voltage as a consumer for the following purposes:

- To verify the source provided voltage is within range after reception of the PS_RDY message and before asserting the **PD_GOOD** signal.
- To monitor for occurrence of overvoltage or undervoltage exception conditions for the negotiated contract, upon which **PD_GOOD** will be de-asserted.

#### 3.4.1.1 Power Supply Transitions

Using **VMON**, the device monitors the voltage on VBUS to manage the transitions of the supply output. The supply power-on and power-off transitions are determined to be at their final states when reaching predefined voltage thresholds, as detailed in Table 3-4. The power-on threshold indicates when the supply has reached the defined voltage. The power-off threshold indicates when the supply output is discharged. All voltage transitions are bound by an internal timer. If the voltage transition times out, the **FAULT_N** pin will be asserted until the power transition is successfully completed.

**TABLE 3-4: VMON POWER-ON/OFF TRANSITION THRESHOLDS**

| | Voltage Threshold (V) | | |
|---|---|---|---|
| | **Min.** | **Typical** | **Max** |
| **Power-On** | - | 3 | - |
| **Power-Off** | - | 2 | - |

#### 3.4.1.2 Overvoltage Condition

Using **VMON**, the device monitors the voltage on VBUS to detect an overvoltage condition on the supply output. The overvoltage condition is determined when the predefined overvoltage threshold is crossed, as detailed in Table 3-5. The **VSELx_N** pins are used to set the overvoltage protection (OVP) voltage on the **VMON** pin. The OVP fault will trigger when the measured voltage on **VMON** is 10% above the selected voltage setting.

On the occurrence of the overvoltage condition:

- The supply output will turned off and discharged.
- The **FAULT_N** pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, **FAULT_N** will be strobed approximately every 5 seconds.

**TABLE 3-5: VMON OVERVOLTAGE THRESHOLDS**

| | Voltage Threshold (V) | | |
|---|---|---|---|
| | **Min.** | **Typical** | **Max** |
| **5 V** | - | 6.0 | 6.9 |
| **9 V** | - | 10.4 | 12.0 |
| **12 V** | - | 13.7 | 15.8 |
| **16 V** | - | 18.1 | 20.9 |
| **20 V** | - | 22.5 | 26.9 |

#### 3.4.1.3 Undervoltage Condition

Using **VMON**, the device monitors the voltage on VBUS to detect an undervoltage condition on the supply output. The undervoltage condition is determined when the predefined undervoltage threshold is crossed, as detailed in Table 3-6. On the occurrence of the undervoltage condition:

- The supply output will turned off and discharged.
- The **FAULT_N** pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, **FAULT_N** will be strobed approximately every 5 seconds.

**TABLE 3-6: VMON UNDERVOLTAGE THRESHOLDS**

| | Voltage Threshold (V) | | |
|---|---|---|---|
| | **Min.** | **Typical** | **Max** |
| **5 V** | - | 4.5 | - |
| **9 V** | - | 8.1 | - |
| **12 V** | - | 10.8 | - |
| **16 V** | - | 14.4 | - |
| **20 V** | - | 18.0 | - |

### 3.4.2 IMON

The integrated current monitor utilizes the **IMON** pin to read a voltage representation of the power supply output current. This pin should be fed by a current sense amplifier tuned to output 3.0 V when 6.0 A is flowing on VBUS. On connection of a port partner and the completion of a negotiated power contract, the overcurrent threshold is set based on the negotiated current. When the device is not connected to a port partner, the overcurrent threshold will be set to the default level. On the occurrence of an overcurrent condition:

- The supply output will turned off and discharged.
- The **FAULT_N** pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, **FAULT_N** will be strobed approximately every 5 seconds.

**TABLE 3-7: IMON OVERCURRENT THRESHOLDS**

| Negotiated Profile Current | Overcurrent Threshold (A) | | |
|---|---|---|---|
| | Min. | Typical | Max |
| **1.5 A** | - | 1.73 | 1.95 |
| **2 A** | - | 2.30 | 2.60 |
| **3 A** | - | 3.45 | 3.90 |
| **5 A** | - | 5.75 | 6.50 |

**Note:** Only sourced currents (when the PD port is operating as a provider) can be monitored by **IMON**. If it is desired to monitor a sinking current (when the port is operating as a consumer), an external circuit should be used and the condition indicated to the device via the **FAULT_IN_N** pin.

## 3.5 SPI ROM Controller

The device is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

**Note:** Microchip suggests using the SST 25 series serial flash family, such as the SST25VF064C.

### 3.5.1 OPERATION OF THE HI-SPEED READ SEQUENCE

The SPI controller will automatically handle code reads going out to the SPI ROM Address. When the controller detects a read, the controller drops the **SPI_ROM_CE_N**, and puts out a 0x0B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next eight clocks clock in the first byte. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_ROM_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

**FIGURE 3-2: SPI ROM HI-SPEED READ OPERATION**

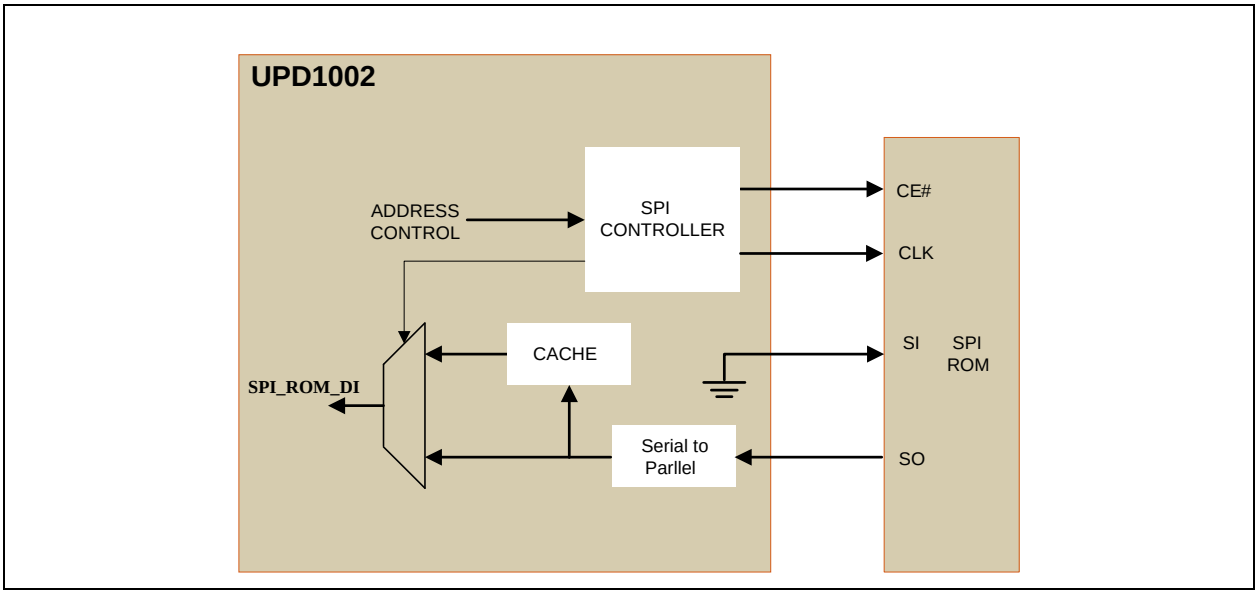
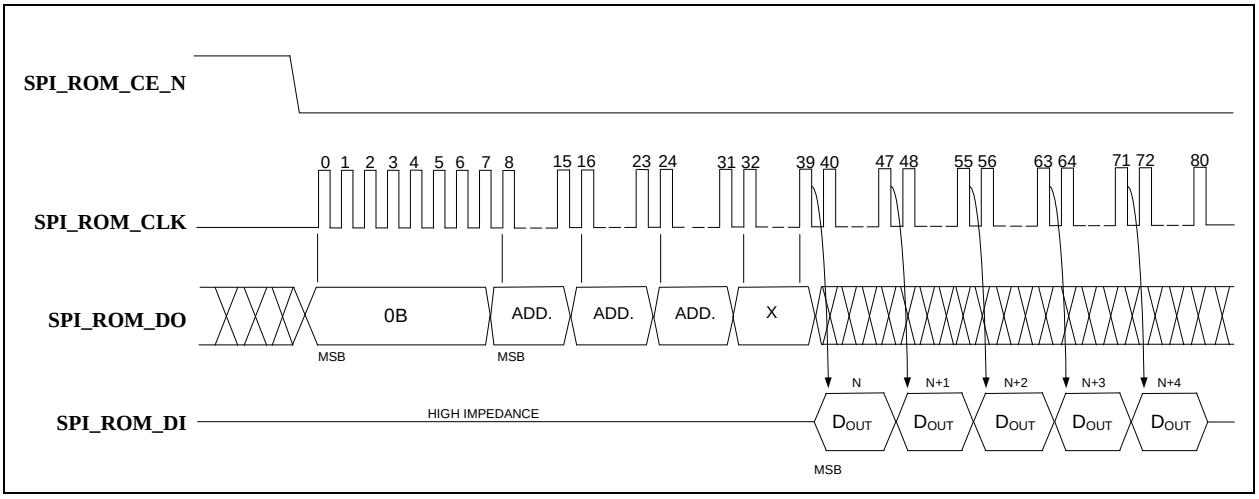


**FIGURE 3-3: SPI ROM HI-SPEED READ SEQUENCE**




## 3.5.2 OPERATION OF THE DUAL HI-SPEED READ SEQUENCE

The SPI controller also supports dual data mode (at 30 MHz SPI speed only). When configured in dual mode, the SPI controller will automatically handle reads going out to the SPI ROM. When the controller detects a read, the controller drops the **SPI_ROM_CE_N**, and puts out a 0x3B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next four clocks clock in the first byte. The data appears two bits at a time on data out and data in. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, the address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_ROM_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

**FIGURE 3-4: SPI ROM DUAL HI-SPEED READ OPERATION**

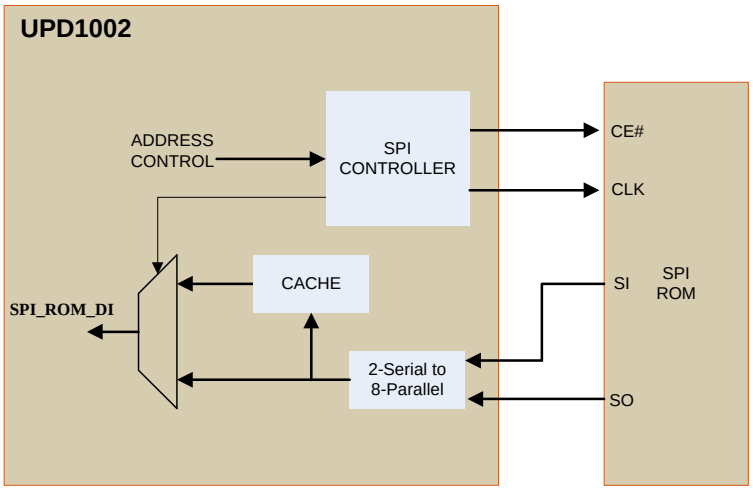
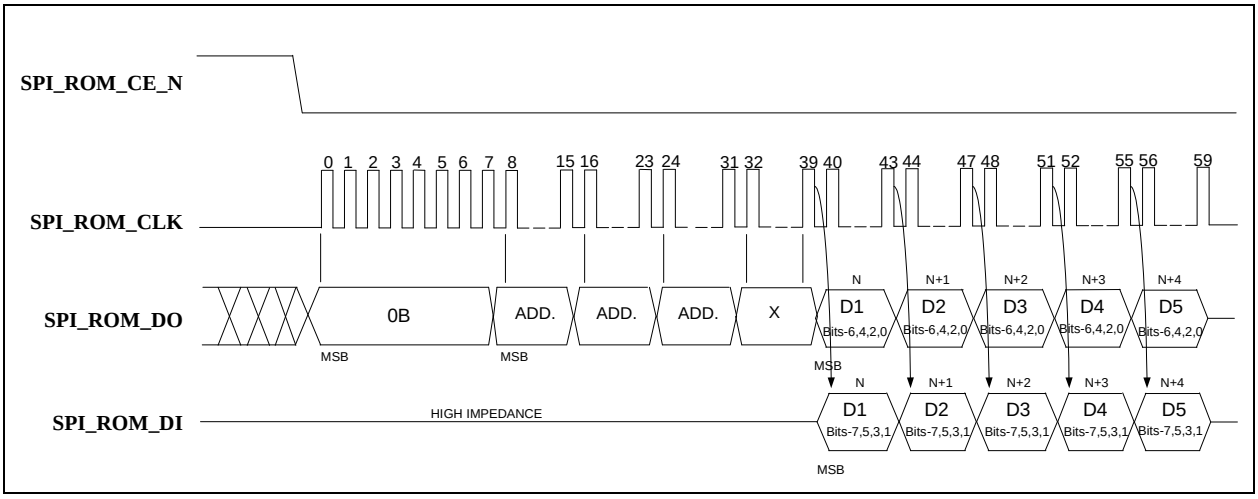


**FIGURE 3-5: SPI ROM DUAL HI-SPEED READ SEQUENCE**



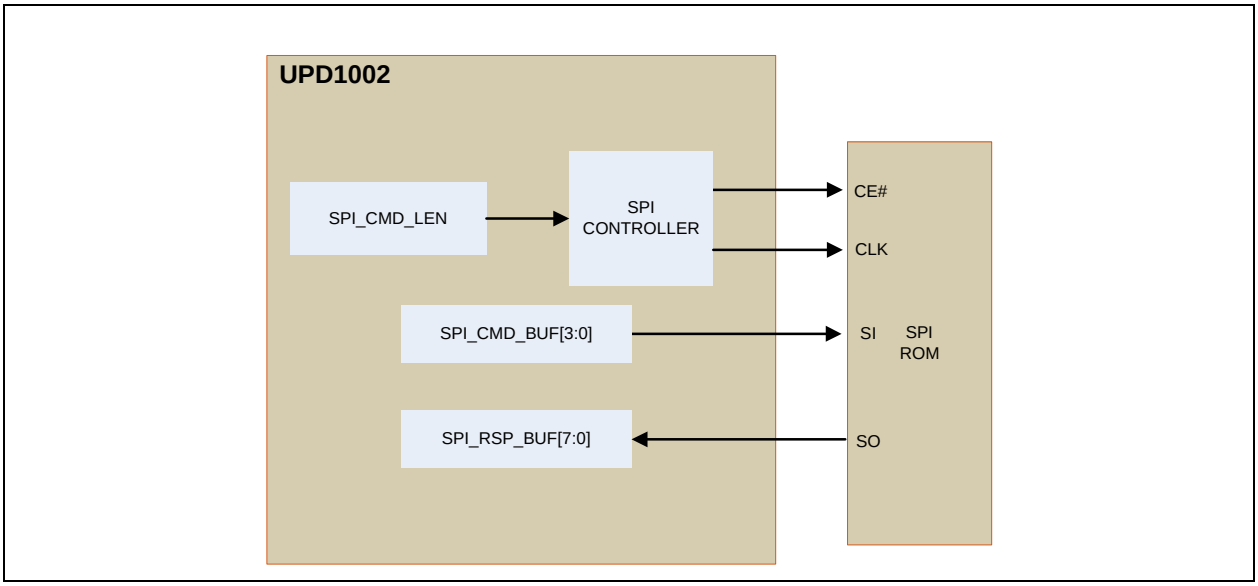

## 3.5.3 32-BYTE CACHE

There is a 32-byte pipeline cache, and associated with the cache is a base address pointer and a length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache, and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the device does a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

## 3.5.4 INTERFACE OPERATION TO SPI PORT WHEN NOT PERFORMING FAST READS

There is an 8-byte command buffer: SPI_CMD_BUF[7:0]; an 8-byte response buffer: SPI_RESP_BUF[7:0]; and a length register that counts out the number of bytes: SPI_CMD_LEN. Additionally, there is a self-clearing GO bit in the SPI_CTL Register. Once the GO bit is set, the device drops **SPI_ROM_CE_N**, and starts clocking. It will put out SPI_CMD_LEN X 8 number of clocks. After the first byte, the COMMAND, has been sent out, and the **SPI_ROM_DI** is stored in the SPI_RESP buffer. If the SPI_CMD_LEN is longer than the SPI_CMD_BUF, don't cares are sent out on the **SPI_ROM_DO** line. This mode is used for program execution out of internal RAM or ROM.

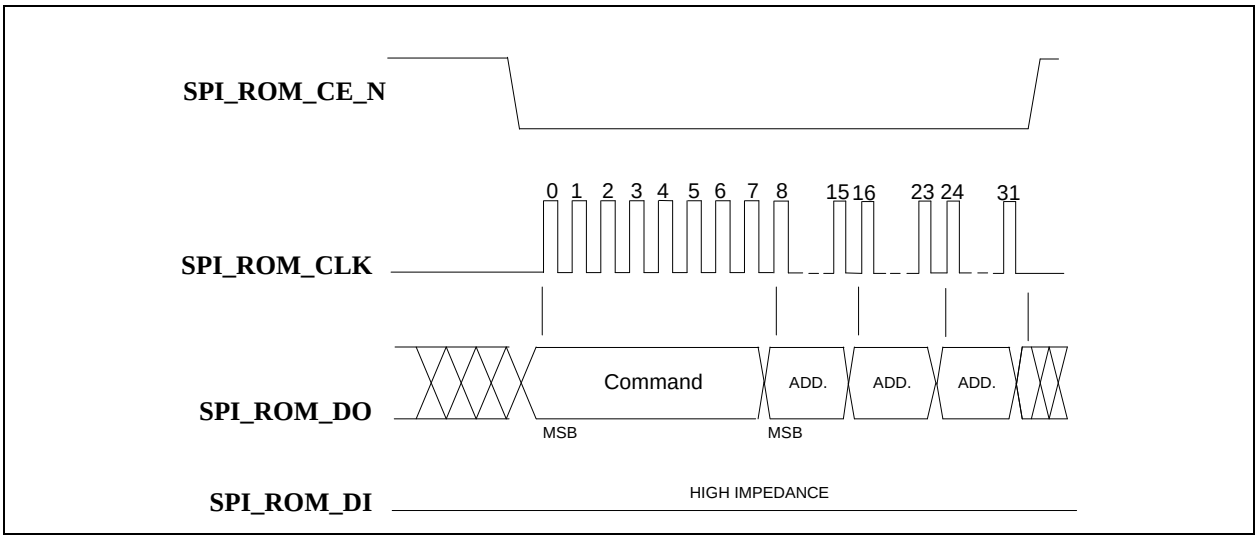
**FIGURE 3-6: SPI ROM INTERNALLY-CONTROLLED OPERATION**



### 3.5.4.1 Erase Example

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To do this, the device first drops **SPI_ROM_CE_N**, then counts out 8 clocks. It then puts out the 8 bits of command, followed by 24 bits of address of the location to be erased on the **SPI_ROM_DO** pin. When the transfer is complete, the **SPI_ROM_CE_N** goes high, while the **SPI_ROM_DI** line is ignored in this example.

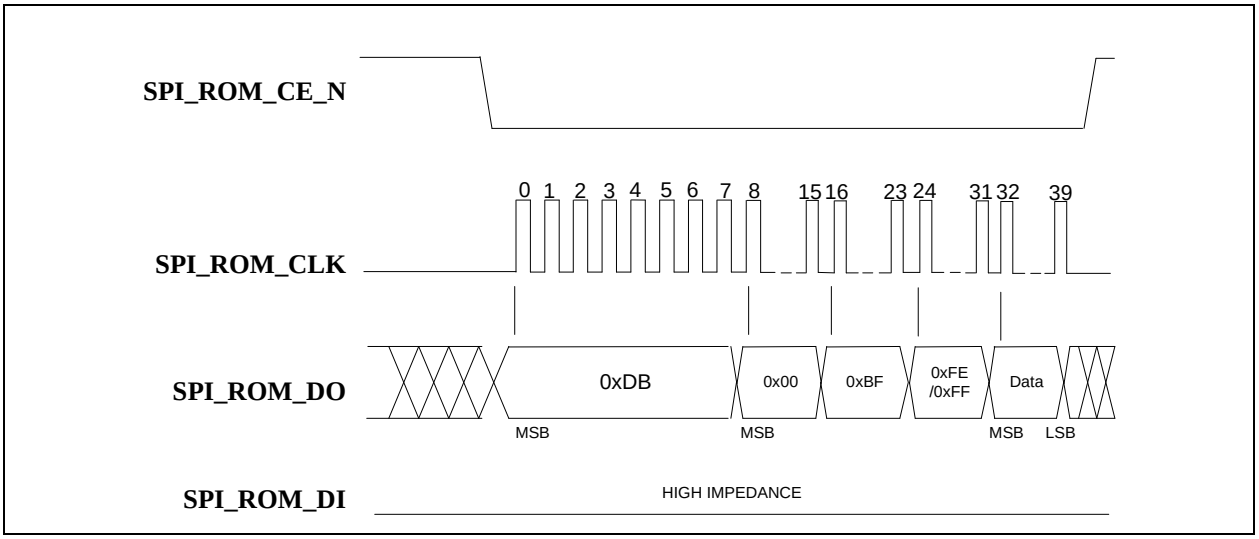
**FIGURE 3-7: SPI ROM ERASE SEQUENCE**




### 3.5.4.2 Byte Program Example

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drops **SPI_ROM_CE_N**, 8 bits of command are clocked out, followed by 24 bits of address, and one byte of data on the **SPI_ROM_DO** pin. The **SPI_ROM_DI** line is not used in this example.

**FIGURE 3-8: SPI ROM BYTE PROGRAM**



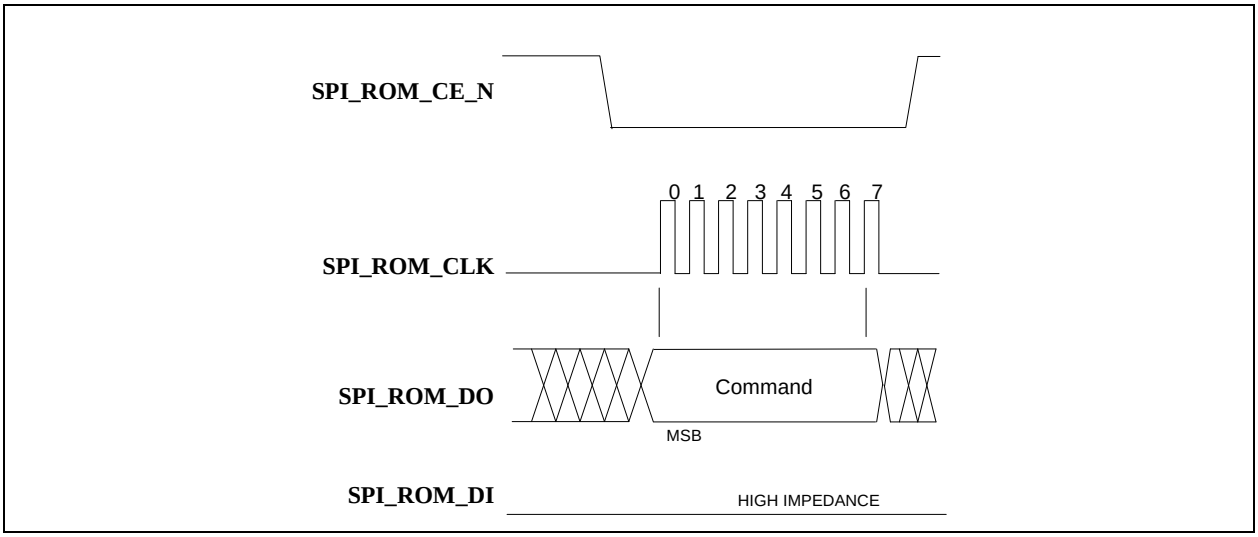
### 3.5.4.3 Command Only Program Example

To perform a single byte command such as the following:

- WRDI
- WREN
- EWSR
- CHIP_ERASE
- EBSY
- DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drops **SPI_ROM_CE_N**, then 8 bits of the command are clocked out on the **SPI_ROM_DO** pin. The **SPI_ROM_DI** is not used in this example.

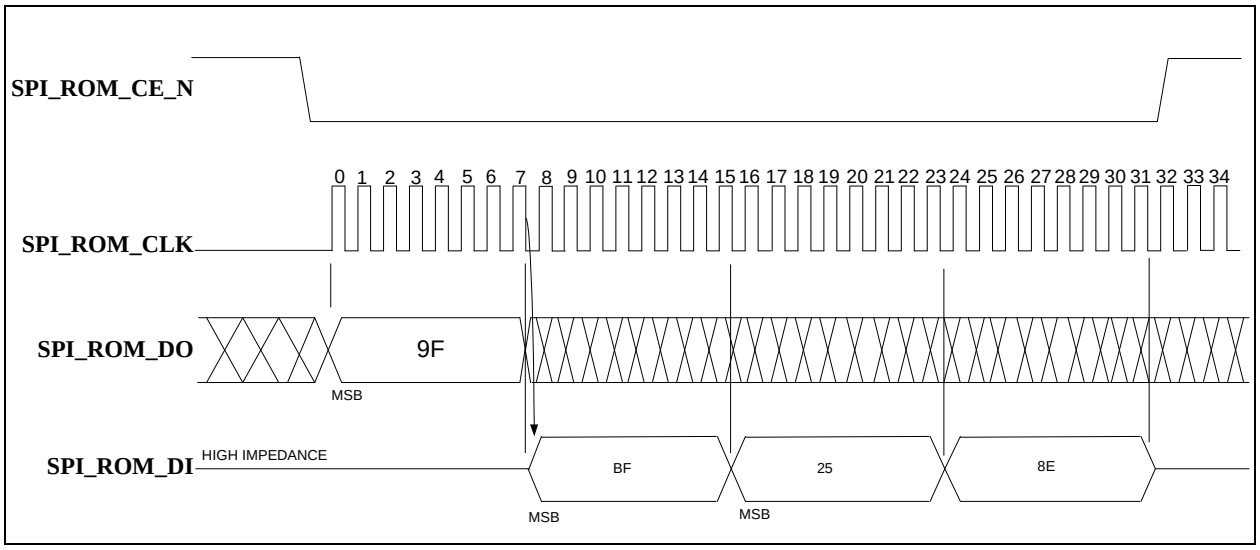
**FIGURE 3-9: SPI ROM COMMAND ONLY SEQUENCE**



### 3.5.4.4 JEDEC-ID Read Example

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF and the length of the transfer is 4 bytes. The device first drops **SPI_ROM_CE_N**, then 8 bits of the command are clocked out, followed by the 24 bits of dummy bytes (due to the length being set to 4) on the **SPI_ROM_DO** pin. When the transfer is complete, the **SPI_ROM_CE_N** goes high. After the first byte, the data on **SPI_ROM_DI** is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

**FIGURE 3-10: SPI ROM JEDEC-ID SEQUENCE**



# 4.0 OPERATIONAL CHARACTERISTICS

## 4.1 Absolute Maximum Ratings*

Supply Voltage (**VDDIO**, **VTR**) (Note 1) . . . . . 0 V to +6.0 V

Positive voltage on input signal pins, with respect to ground . . . . . +6.0 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Storage Temperature . . . . . -55$^{o}$C to +150$^{o}$C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . +/-2 kV

**Note 1:** When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 4.2, "Operating Conditions**", Section 4.4, "DC Specifications", or any other applicable section of this specification is not implied.

## 4.2 Operating Conditions**

Supply Voltage (**VTR**) . . . . . +3.1 V to +5.3 V

Supply Voltage (**VDDIO**) . . . . . +3.1 V to +3.47 V

Positive voltage on input signal pins, with respect to ground . . . . . +3.3 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.3 V

Positive voltage on **VMON** and **IMON** pins, with respect to ground . . . . . VDDIO

Negative voltage on **VMON** and **IMON** pins, with respect to ground . . . . . -0.3 V

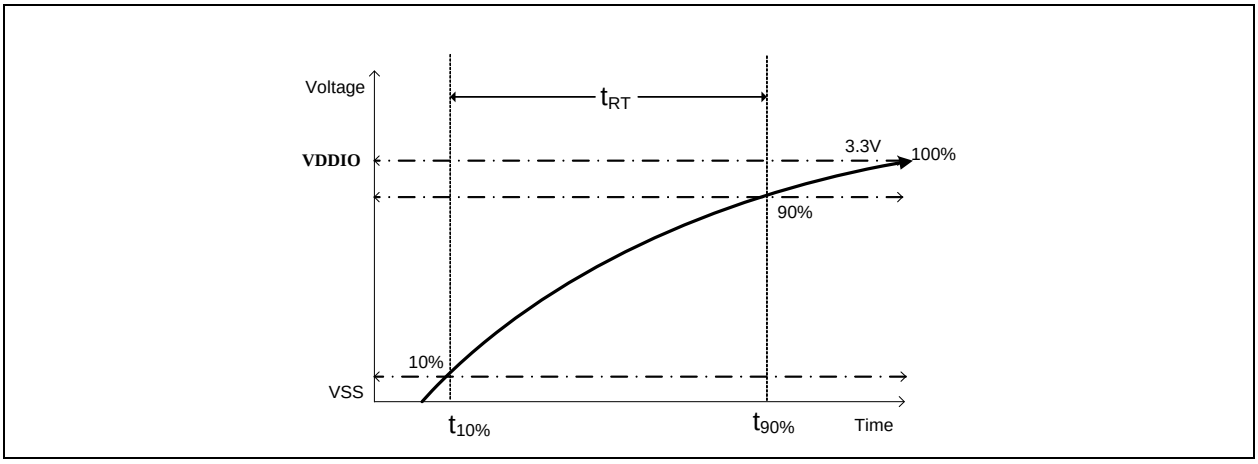
Power Supply Rise Time Max $t_{RT}$ (Figure 4-1) . . . . . TBD

Ambient Operating Temperature in Still Air ($T_A$) . . . . . Note 2

**Note2:** 0$^{o}$C to +70$^{o}$C for commercial version, -40$^{o}$C to +85$^{o}$C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

**FIGURE 4-1: SUPPLY RISE TIME MODEL**



## 4.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

**Note:** Maximum values represent very short bursts of activity over a small amount of time. Typical values represent averaged current consumption over time.

**TABLE 4-1: DEVICE POWER CONSUMPTION**

| Power State | VTR Supply Current | | |
|---|---|---|---|
| | Typical | Max | Units |
| **RESET** | 0.325 | 3.5 | mA |
| **PROVIDER MODE** | | | |
| **Wait Insert State** | 1.2 | 16.2 | mA |
| **Legacy Device Connected** | 14.6 | 58.5 | mA |
| **PD Device Connected** | 28.0 | 69.0 | mA |
| **CONSUMER MODE** | | | |
| **Sink Discovery State / Legacy Device Connected** | 10.0 | 45.0 | mA |
| **PD Device Connected** | 28.0 | 69.0 | mA |

## 4.4 DC Specifications

**TABLE 4-2: DC ELECTRICAL CHARACTERISTICS**

| Parameter | Symbol | Min | Typ | Max | Units | |
|---|---|---|---|---|---|---|
| **IS Type Input Buffer** | | | | | | |
| Low Input Level | $V_{ILI}$ | -0.3 | | 0.8 | V | |
| High Input Level | $V_{IHI}$ | 2.5 | | **VDDIO**+0.3 | V | |
| Negative-Going Threshold | $V_{ILT}$ | 1.25 | 1.35 | 1.55 | V | Schmitt trigger |
| Positive-Going Threshold | $V_{IHT}$ | 1.40 | 1.65 | 1.76 | V | Schmitt trigger |
| Schmitt Trigger Hysteresis ($V_{IHT}$ - $V_{ILT}$) | $V_{HYS}$ | 188 | 225 | 250 | mV | |
| Input Leakage ($V_{IN}$ = **VSS** or **VDDIO**) | $I_{IH}$ | -9.79 | | 7.14 | nA | Note 3 |
| Input Capacitance | $C_{IN}$ | | | 3 | pF | |
| **O8 Type Buffers** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.35 | V | $I_{OL}$ = -8 mA |
| High Output Level | $V_{OH}$ | **VDDIO** - 0.7 | | | V | $I_{OH}$ = 8 mA |
| **OD8 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.35 | V | $I_{OL}$ = -8 mA |

**Note3:** This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 µA per-pin (typical).

## 4.5 AC Specifications

This section details the various AC timing specifications of the device.

### 4.5.1 RESET TIMING

Figure 4-2 illustrates the **RESET_N** timing requirements. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified.

Refer to Section 3.1, "Resets," on page 23 for additional information on resets.

**FIGURE 4-2: RESET_N TIMING**

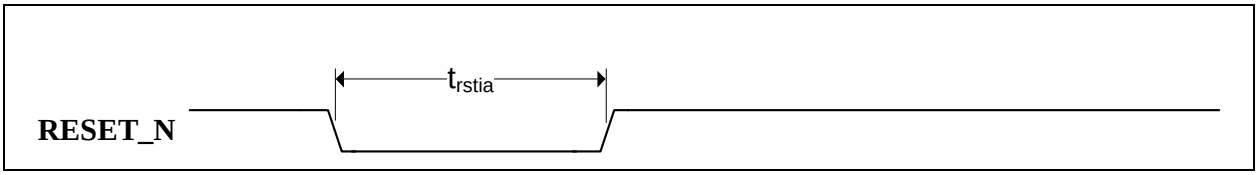



**TABLE 4-3: RESET_N TIMING**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{rstia}$ | **RESET_N** input assertion time | 1 | | | µs |

### 4.5.2 SPI ROM CONTROLLER TIMING

The following specifies the SPI ROM Controller timing requirements for the device.

**FIGURE 4-3: SPI ROM CONTROLLER TIMING**

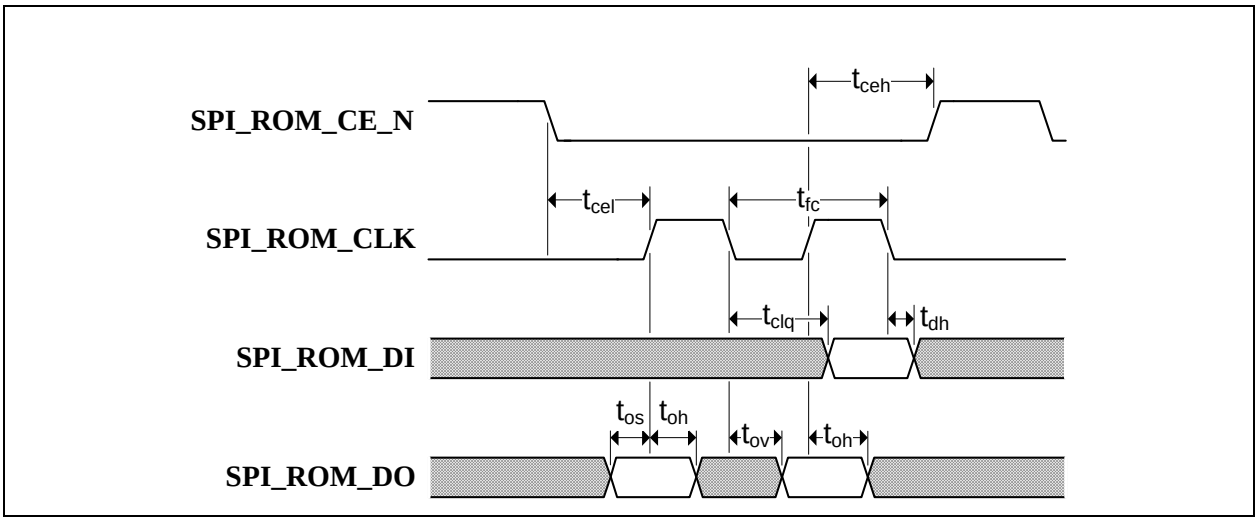



**TABLE 4-4: SPI ROM CONTROLLER TIMING VALUES**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{fc}$ | Clock frequency | 46.86 | 48 | 48.62 | MHz |
| $t_{ceh}$ | Chip enable (**SPI_ROM_CE_EN**) high time | | 50 | | ns |
| $t_{clq}$ | Clock to input data | | 15 | | ns |
| $t_{dh}$ | Input data hold time | 0.70 | 3 | 4.52 | ns |
| $t_{os}$ | Output setup time | 5.35 | 7 | 8.28 | ns |
| $t_{oh}$ | Output hold time | 11.57 | 13 | 15.22 | ns |
| $t_{ov}$ | Clock to output valid | 1.16 | 2 | 3.3 | ns |
| $t_{cel}$ | Chip enable (**SPI_ROM_CE_EN**) low to first clock | | 12 | | ns |
| $t_{ceh}$ | Last clock to chip enable (**SPI_ROM_CE_EN**) high | | 12 | | ns |

### 4.5.3 USB POWER DELIVERY SIGNAL TIMING

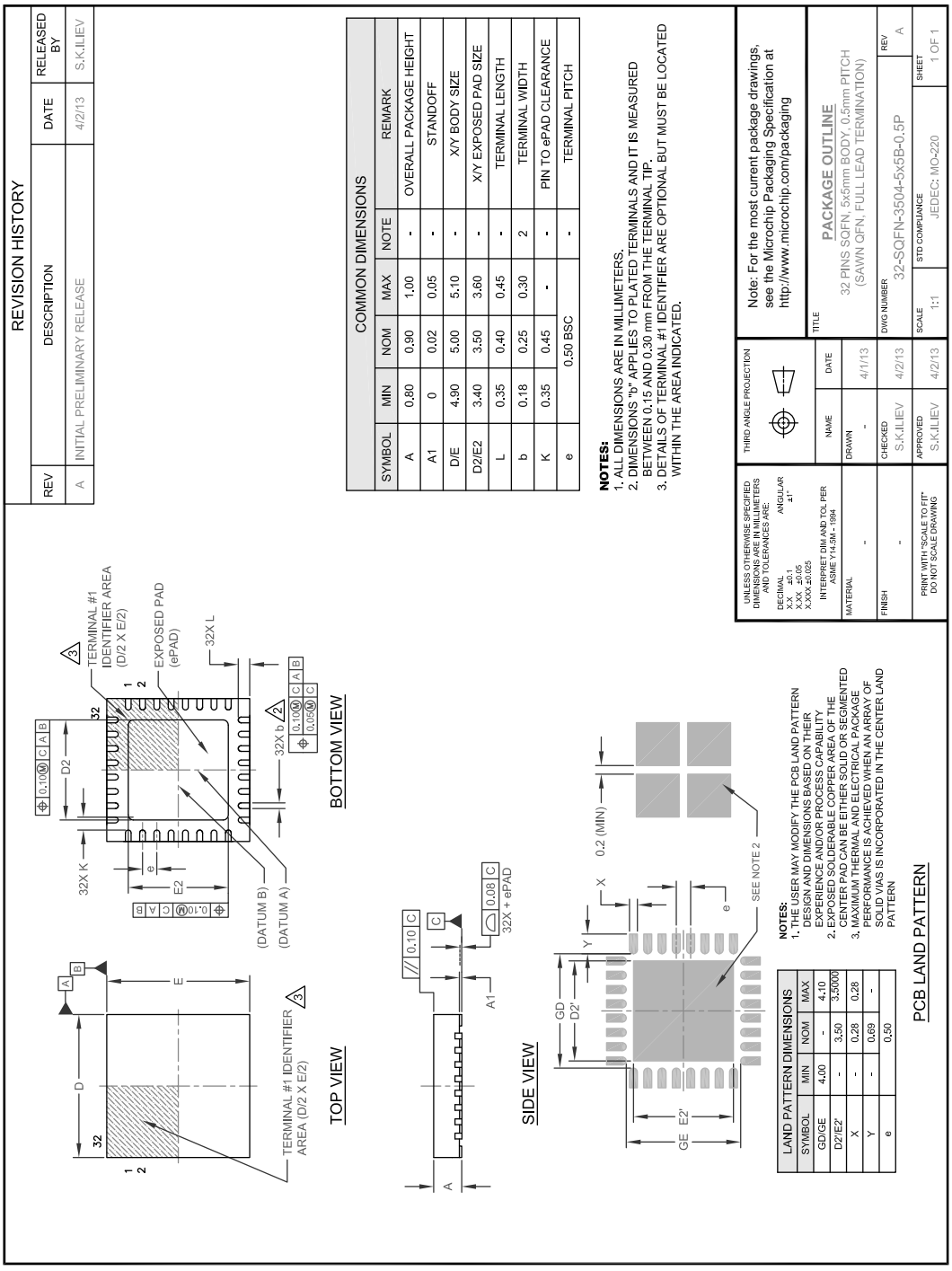
All USB Power Delivery signals (**PD_DATA**, **PD_ID**) conform to the voltage, power, and timing characteristics/specifications as set forth in the USB Power Delivery Specification. Please refer to the *USB Power Delivery Specification*, available at http://www.usb.org.

## 5.0 PACKAGE OUTLINE

### 5.1 32-SQFN

**Note:** For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

**FIGURE 5-1: 32-SQFN PACKAGE**



## 6.0 REVISION HISTORY

**TABLE 6-1: REVISION HISTORY**

| Revision Level & Date | Section/Figure/Entry | Correction |
|---|---|---|
| DS00001760B (12-02-14) | Table 3-4, Table 3-5, Table 3-6, and Table 3-7 | Added IMON/VMON thresholds (was TBD). |
| | Section 4.5, "AC Specifications," on page 39 | Removed “VMON/IMON FAULT RECOVERY TIMING” and “FAULT_IN_N RECOVERY TIMING” sections. |
| | Table 3-2, “CFG_SELx PIN Resistor-Capacitor BIN ALLOCATION,” on page 24 | Updated Cx tolerance to +/-5%. |
| | Table 4-1, “Device Power Consumption,” on page 38 | Updated power consumption table. |
| | All: Cover, Intro | Removed “Programmable” from part description. |
| DS00001760A | | Initial Release |

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| PART NO. | [X] | - | XX | / | XX |
|---|---|---|---|---|---|
| Device | Tape and Reel Option | | Temperature Range | | Package |

| | | |
|---|---|---|
| **Device:** | UPD1002 | |
| **Tape and Reel Option:** | Blank<br>T | = Standard packaging (tray)<br>= Tape and Reel(Note 1) |
| **Temperature Range:** | A<br>AI | = 0°C to +70°C (Commercial)<br>= -40°C to +85°C (Industrial) |
| **Package:** | MQ | = 32-pin SQFN |

**Examples:**

a) UPD1002-A/MQ
Tray, Commercial temp., 32-pin SQFN

b) UPD1002T-AI/MQ
Tape & reel, Industrial temp., 32-pin SQFN

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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