
USB Power Delivery Controller

Highlights

- Integrated USB Power Delivery (PD) PHY
- Support for Power Delivery Message Protocol
- Integrated Voltage and Current ADC Inputs
- Configuration Profile Selection
- On-chip Microcontroller
- SPI Interface
- Commercial and Industrial Grade Temperature Support
- Available in 32-SQFN Package

Target Applications

- AC Adapters & Chargers
 - Type-A
 - Type-B
 - Micro-A
 - Micro-B
 - Captive cable

Key Benefits

- Integrated USB Power Delivery (PD) PHY
 - Integrated receive termination
 - Requires minimal external components
- Support for Power Delivery Message Protocol
 - Message Generation/Consumption
 - Retry Generation
 - Error Handling
 - State Behavior
- Cable Detect Logic
 - Cable attachment type
- CFG_SEL pins allow selection of multiple profiles
 - Provider
 - Consumer/Provider
- Integrated Voltage (VMON) and Current (IMON) ADC Inputs
- Dead Battery Support
- On-chip Microcontroller
 - Manages I/Os and other signals
 - Implements power delivery policy engine and device policy manager
- Configuration Programming via OTP, or Vendor Defined Messaging
- Supports Low Power Modes
- Serial Peripheral Interface (SPI) Bus
- Internal 3.3 V and 1.8 V Voltage Regulators
- Integrated Oscillator Reduces BOM Costs
- Package
 - 32-pin SQFN (5 x 5 mm)
- Environmental
 - Commercial temperature range (0°C to +70°C)
 - Industrial temperature range (-40°C to +85°C)

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UPD1001

1.0 INTRODUCTION

1.1 General Description

The UPD1001 is a USB Power Delivery (PD) controller designed to adhere to the *USB Power Delivery Specification*. USB Power Delivery allows a host (or device) to provide or consume up to 5 Amps and/or up to 20 Volts of power from a USB PD capable partner device on the other end of the USB cable. USB PD capable standard and custom cables/connectors are supported, which in most cases are backward compatible with standard USB connections.

The UPD1001 provides a complete USB Power Delivery solution for all charger and adapter solutions. The functionality of the UPD1001 is selected via two configuration selection pins, **CFG_SEL0** and **CFG_SEL1**, which can be used to select unique PD and system configurations. Designing the UPD1001 into a system can be as simple as selecting a configuration, with no external EEPROM required. Advanced programmability options exist with an external EEPROM installed.

The integrated USB Power Delivery MAC and PHY support provider and consumer operation via the PD communication protocol, as specified in Revision 1.0 (Version 1.2) of the *USB Power Delivery Specification*. Monitoring of VBUS and battery charging is accomplished via the integrated voltage and current ADC inputs. The PHY supports cable ID detection/identification and loopback modes. The PHY includes a 24MHz FSK modulator/demodulator and provides integrated terminations. The USB PD MAC supports both USB PD insertion detection (cold socket) and dead battery cases.

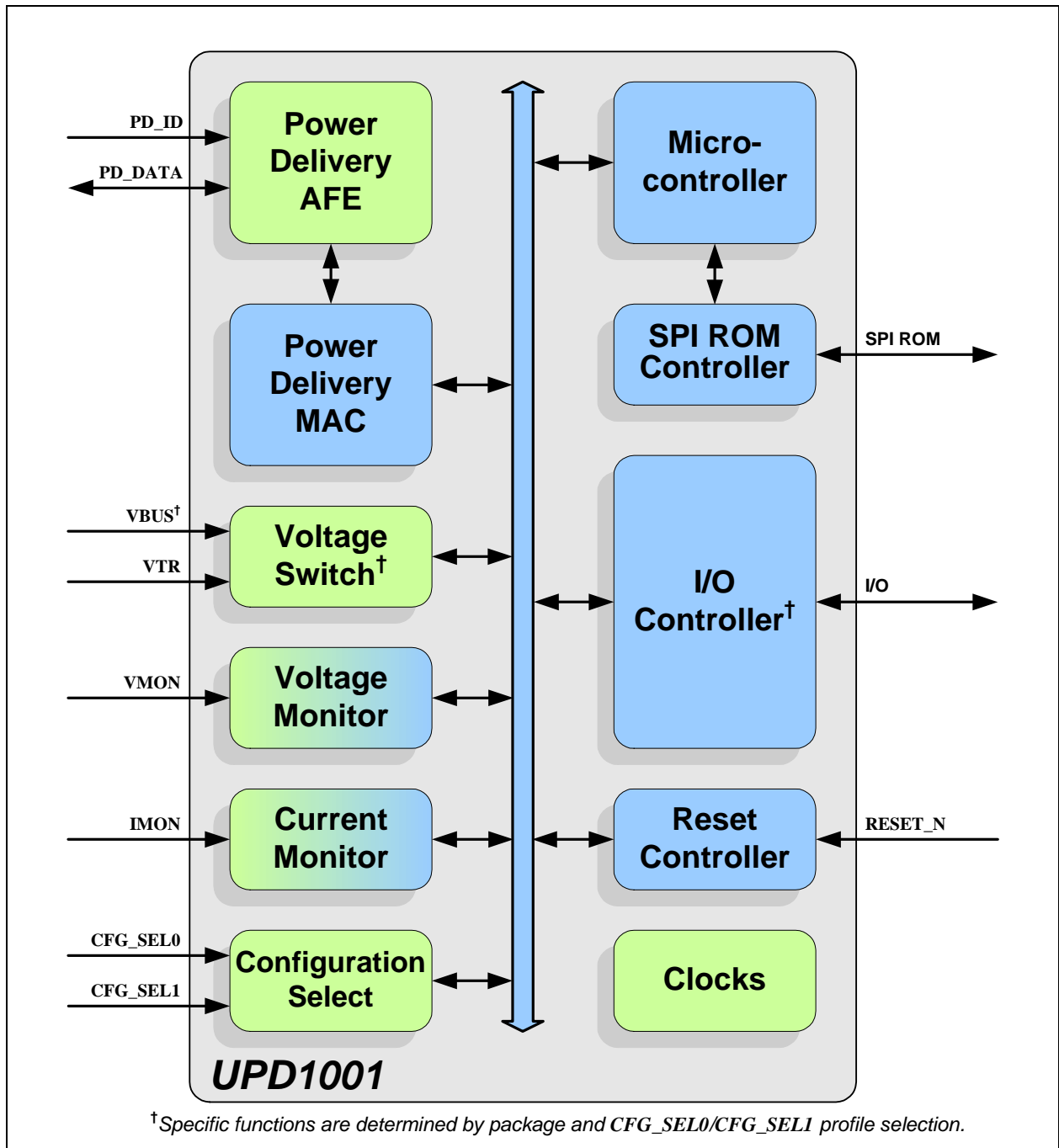
The on-chip microcontroller manages the IOs and implements the power delivery local policy engine and device manager. The SPI ROM controller is used by the microcontroller for optional external code execution from ROM. A One Time Programmable (OTP) ROM is integrated in the UPD1001. Integrated 3.3 V and 1.8 V regulators allow device operation from a single power supply. The UPD1001 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the UPD1001 is shown in [Figure 1-1](#).

The UPD1001 is offered in a 32-pin SQFN package. The package provides multiple pin configurations, based upon the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals. [Table 1-1](#) summarizes the available pin combinations and their target applications. Refer to [Section 2.0, "Pin Descriptions and Configuration," on page 6](#) for detailed information on specific pin configurations.

TABLE 1-1: UPD1001 PACKAGE/PIN CONFIGURATION SUMMARY

Package	Pin Config. Name	PD Role	USB Receptacle	Notes
32-SQFN	32-A	Provider	Standard-A (STD-A)	See Section 2.1 for pin assignments
	32-B	Consumer/Provider	Standard-B (STD-B)	See Section 2.1 for pin assignments

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



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2.0 PIN DESCRIPTIONS AND CONFIGURATION

The pinouts for the package, along with system-level application diagrams, are detailed in the following section:

- [32-Pin SQFN \(32-SQFN\)](#)

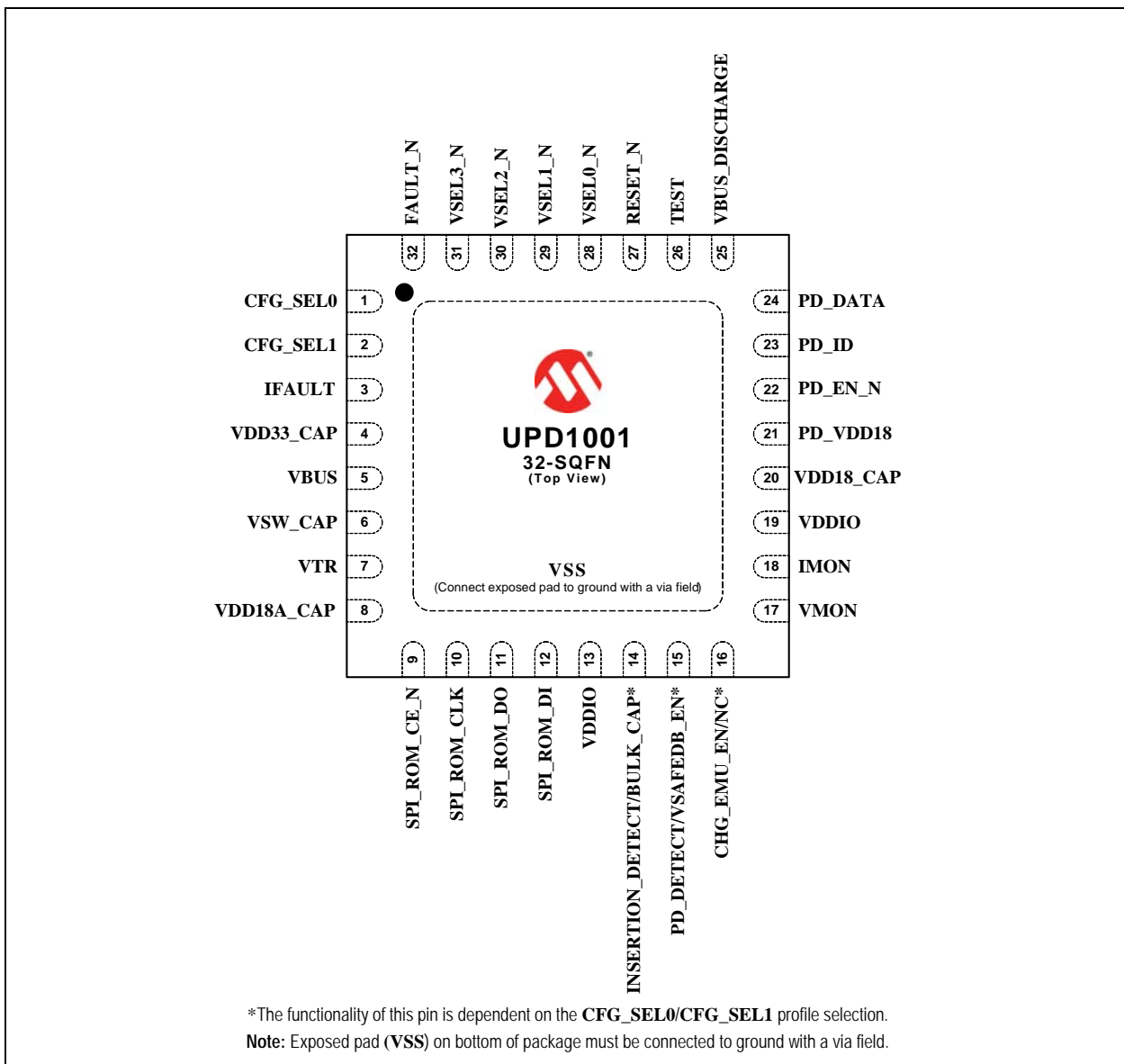
Note: For a summary of the available pin combinations and their corresponding target applications, refer to [Table 1-1](#).

Pin descriptions are detailed in [Section 2.2, "Pin Descriptions," on page 10](#). For details on the **CFG_SEL0** and **CFG_SEL1** Configuration Select signals, refer to [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)," on page 20](#).

2.1 32-Pin SQFN (32-SQFN)

2.1.1 32-SQFN PIN DIAGRAM

FIGURE 2-1: 32-SQFN PIN ASSIGNMENTS (TOP VIEW)



Note: When an “_N” is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column of [Table 2-2, "Pin Descriptions"](#). A description of the buffer types is provided in [Section 2.3, "Buffer Types"](#).

2.1.2 32-SQFN PIN ASSIGNMENTS

The UPD1001 32-SQFN provides two distinct pin configurations (32-A and 32-B) based upon the **CFG_SEL0** and **CFG_SEL1** Configuration Select pins. The 32-A and 32-B pin configurations are designed for use with USB Standard-A and Standard-B receptacles, respectively, and are detailed in [Table 2-1](#). For pin descriptions, refer to [Section 2.2, "Pin Descriptions"](#). For example connection diagrams, refer to [Section 2.4, "Power Connection Diagram,"](#) on page 18. For information on the Configuration Select pins, refer to [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)"](#).

Note: The 32-A and 32-B pin configuration assignments differ only on pins 14, 15, and 16.

TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS

Pin Number	Configuration 32-A Name	Configuration 32-B Name
1	CFG_SEL0	
2	CFG_SEL1	
3	IFault	
4	VDD33_CAP	
5	VBUS	
6	VSW_CAP	
7	VTR	
8	VDD18A_CAP	
9	SPI_ROM_CE_N	
10	SPI_ROM_CLK	
11	SPI_ROM_DO	
12	SPI_ROM_DI	
13	VDDIO	
14	INSERTION_DETECT	BULK_CAP
15	PD_DETECT	SAFEDB_EN
16	CHG_EMU_EN	NC
17	VMON	
18	IMON	
19	VDDIO	
20	VDD18_CAP	
21	PD_VDD18	
22	PD_EN_N	
23	PD_ID	
24	PD_DATA	
25	VBUS_DISCHARGE	
26	TEST	
27	RESET_N	
28	VSEL0_N	

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TABLE 2-1: 32-SQFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	Configuration 32-A Name	Configuration 32-B Name
29	VSEL1_N	VSEL1_N
30	VSEL2_N	VSEL2_N
31	VSEL3_N	VSEL3_N
32	FAULT_N	FAULT_N
Exposed Pad	VSS	VSS

2.1.3 32-SQFN SYSTEM LEVEL DIAGRAMS

Figure 2-2 and Figure 2-3 provide typical system level diagrams of the UPD1001 for 32-A (Standard-A receptacle) and 32-B (Standard-B receptacle) applications, respectively.

FIGURE 2-2: CONFIGURATION 32-A SYSTEM-LEVEL DIAGRAM

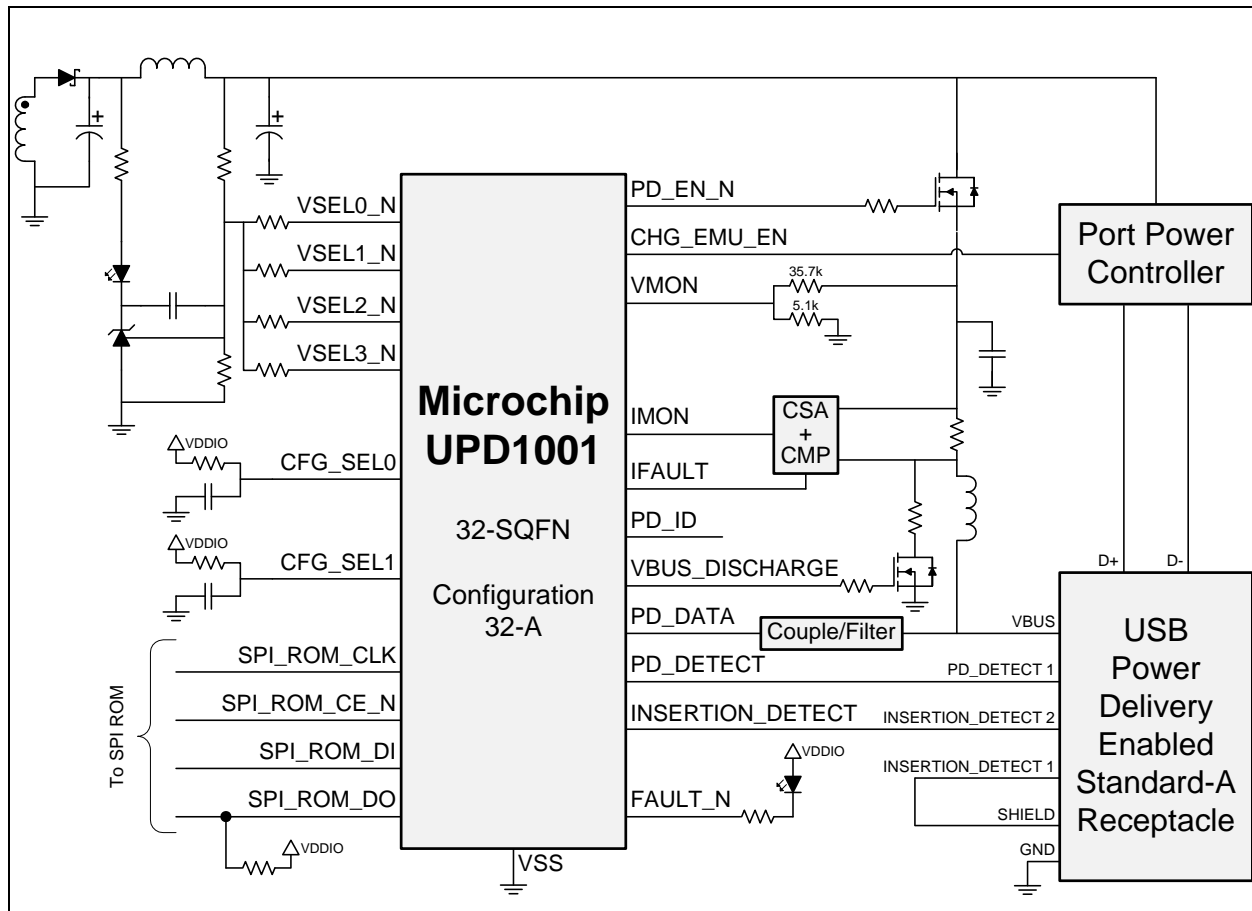
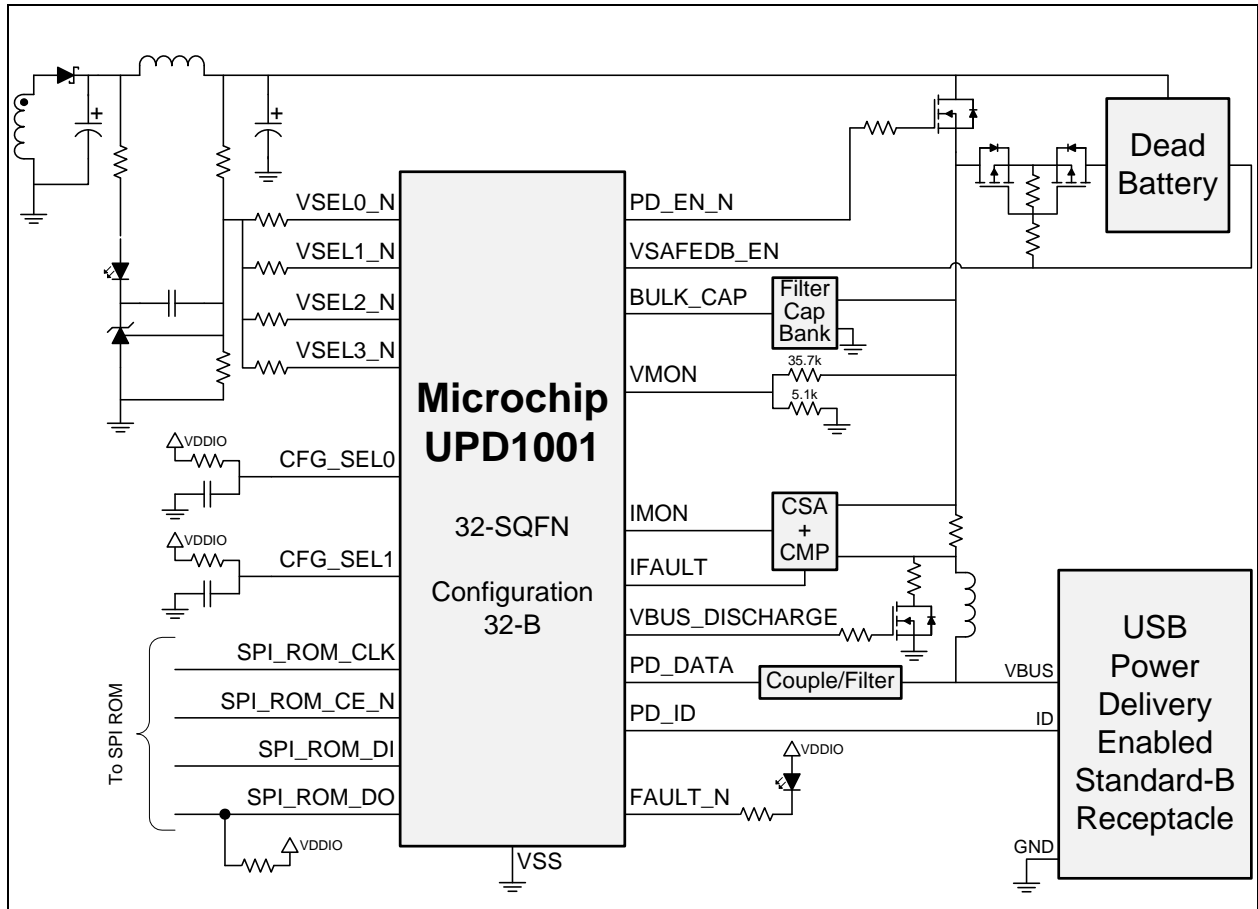


FIGURE 2-3: CONFIGURATION 32-B SYSTEM-LEVEL DIAGRAM



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2.2 Pin Descriptions

TABLE 2-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Power Delivery			
Power Delivery Cable ID	PD_ID	AIO	USB connector signal used to indicate a high-current power delivery capable cable is inserted. This signal is to be connected to the PD_ID pin located on the USB PD Standard-B receptacle.
Power Delivery VBUS Data	PD_DATA	AIO	Modulated power delivery VBUS data. Requires in-line isolation filter. Reference schematic available on request.
Power Delivery Detect	PD_DETECT	IS (PU)	This signal is to be connected to the PD DETECT pins located on the USB PD Standard-A receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) of PD_DETECT qualifies a USB-PD plug detection event. Note: This function is only available in specific device configurations.
Power Delivery Enable	PD_EN_N	O8	This active low signal controls output of the power supply voltage onto VBUS. This signal will typically always be asserted, even when VBUS is 5 V.
Miscellaneous			
VBUS Voltage Monitor	VMON	AI	Stepped down voltage representation of the VBUS voltage. This signal must be connected to a voltage divider circuit as specified in Section 2.4, "Power Connection Diagram," on page 18. Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 25 for additional information.
Charger Current Monitor	IMON	AI	Voltage representation of the charger current. This signal should be fed by a current sense amplifier tuned to output 3.0 V when 6.0 A is flowing on VBUS. Voltage must not exceed 5 V on this signal. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 25 for additional information.
Power Supply Fault Indicator	FAULT_N	OD8	This active low signal can be connected to an external LED or SoC and is used by the device to indicate power supply exceptions/failures as determined by the integrated voltage/current monitors. Refer to Section 3.4, "Voltage/Current Monitors (VMON/IMON)," on page 25 for additional information.
Power Delivery Profile Configuration Selector 0	CFG_SEL0	AIO	This pin is used in conjunction with CFG_SEL1 to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information.

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description																														
Power Delivery Profile Configuration Selector 1	CFG_SEL1	AIO	<p>This pin is used in conjunction with CFG_SEL0 to select the power delivery profile of the device via an externally connected RC circuit. Refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)" for additional information.</p>																														
Source Voltage Select 0	VSEL0	OD8	<p>This pin is used in conjunction with VSEL1 to select the correct source voltage from the DC-to-DC or AC-to-DC solution. VSEL1 and VSEL0 select the voltage value from the supported voltage capabilities in ascending order with VSEL0 being the least significant bit (see examples below).</p> <p>For example, if an adapter supports 5, 9, and 20 V capabilities, the VSEL1 and VSEL0 selections will be as follows:</p> <table border="0" data-bbox="833 821 1161 961"> <tr> <td colspan="3">VSEL1 VSEL0</td> </tr> <tr> <td>0</td> <td>0:</td> <td>5 V</td> </tr> <tr> <td>0</td> <td>1:</td> <td>9 V</td> </tr> <tr> <td>1</td> <td>0:</td> <td>20 V</td> </tr> <tr> <td>1</td> <td>1:</td> <td>RESERVED</td> </tr> </table> <p>In another example, if an adapter supports 5, 9, 12, and 20 V capabilities, the VSEL1 and VSEL0 selections will be as follows:</p> <table border="0" data-bbox="833 1115 1079 1255"> <tr> <td colspan="3">VSEL1 VSEL0</td> </tr> <tr> <td>0</td> <td>0:</td> <td>5 V</td> </tr> <tr> <td>0</td> <td>1:</td> <td>9 V</td> </tr> <tr> <td>1</td> <td>0:</td> <td>12 V</td> </tr> <tr> <td>1</td> <td>1:</td> <td>20 V</td> </tr> </table> <p>For a mapping of the VSEL1/VSEL0 voltage assignments for each CFG_SEL1/CFG_SEL0 configuration profile, refer to TABLE 3-3: 32-SQFN CFG_SELx Configuration Assignments on page 21.</p> <p>Note: This function is only available in specific device configurations.</p>	VSEL1 VSEL0			0	0:	5 V	0	1:	9 V	1	0:	20 V	1	1:	RESERVED	VSEL1 VSEL0			0	0:	5 V	0	1:	9 V	1	0:	12 V	1	1:	20 V
VSEL1 VSEL0																																	
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0	1:	9 V																															
1	0:	12 V																															
1	1:	20 V																															
Source Voltage Select 1	VSEL1	OD8	<p>This signal is used in conjunction with VSEL0 to select the correct source voltage from the DC-to-DC or AC-to-DC solution. VSEL0 and VSEL1 select the voltage value from the supported voltage capabilities in ascending order.</p> <p>Refer to the VSEL0 definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p>																														

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Source Voltage Select 0	VSEL0_N	OD8	<p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, VSEL2_N, and VSEL3_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>For example, if 5, 12 and 20 V capabilities are supported, the VSELx_N selections will be as follows:</p> <p>VSEL0_N = 5 V VSEL1_N = 12 V VSEL2_N = 20 V VSEL3_N = RESERVED</p> <p>In another example, if only 5 and 20 V are supported, the VSELx_N selections will be as follows:</p> <p>VSEL0_N = 5 V VSEL1_N = 20 V VSEL2_N = RESERVED VSEL3_N = RESERVED</p> <p>The VSELx_N pins are also used to set the overvoltage protection (OVP) voltage on the VMON pin. The OVP fault will trigger when the measured voltage on VMON is 10% above the selected voltage setting.</p> <p>For a mapping of the VSELx_N voltage assignments for each CFG_SEL1/CFG_SEL0 configuration profile, refer to Section 3.3, "Configuration Selection (CFG_SEL0/CFG_SEL1)," on page 20.</p> <p>Note: This function is only available in specific device configurations.</p>
Source Voltage Select 1	VSEL1_N	OD8	<p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, VSEL2_N, and VSEL3_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>Refer to the VSEL0_N definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p>

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Source Voltage Select 2	VSEL2_N	OD8	<p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, VSEL2_N, and VSEL3_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>Refer to the VSEL0_N definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p>
Source Voltage Select 3	VSEL3_N	OD8	<p>This active low signal is one in a series of output pins (VSEL0_N, VSEL1_N, VSEL2_N, and VSEL3_N) used to select the correct source voltage from the DC-to-DC solution. Each VSELx_N pin is dedicated to one voltage, assigned in order of increasing supported voltage.</p> <p>Refer to the VSEL0_N definition for additional information.</p> <p>Note: This function is only available in specific device configurations.</p>
VBUS Discharge	VBUS_DISCHARGE	O8	<p>This active high output is used to drive a power NFET to discharge VBUS during high-to-low voltage transitions in order to achieve vSafe0V. When asserted, the external MOSFET should conduct to GND through a current limiting resistor. This signal de-asserts when the VMON signal voltage reaches a preset value (a percentage of the destination voltage).</p>
Emulation Enable	CHG_EMU_EN	O8	<p>This active high output signal can be used to drive the Emulation Enable pin of a Microchip UCS1001 or similar device that supports BC 1.2. The device will assert this signal whenever operating at VSafe5V without a PD contract. Whenever a PD contract is established (even at 5 V), this signal is de-asserted.</p> <p>Note: This function is only available in specific device configurations.</p>

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Insertion Detect	INSERTION_DETECT	IS (PU)	<p>This active low input signal should be connected to the Insertion Detect pin on the USB Standard-A (STD-A) receptacle. This signal is pulled high via an internal pull-up resistor by default. Assertion (low value) qualifies a STD-A plug insertion event and triggers transition out of the “Startup” state of the Source Policy engine. The device firmware implements cold socket detection using the INSERTION_DETECT signal. Even when operating as a provider, if the signal is high, the device will not output voltage on VBUS. VSafe5V will only be output upon assertion of this signal (low).</p> <p>Note: Cold socket (insertion detect) is an optional feature in the USB PD specification. If this feature is not being used in a design, the INSERTION_DETECT signal must be grounded.</p> <p>Note: This function is only available in specific device configurations.</p>
Dead Battery Enable	VSAFEDB_EN	O8	<p>This active high output signal is used to enable the dead battery supply on a USB Standard-B (STD-B) receptacle (consumer/provider) AC adapter. When no voltage has been detected on VBUS, this signal is asserted every 10 s to back power an attached provider/consumer and determine whether the attached device has specified to be powered per the dead battery mechanisms specified in the PD specification.</p> <p>Note: This function is only available in specific device configurations.</p>
Bulk Capacitance Enable	BULK_CAP	O8	<p>This active high output signal is used to enable/disable the source bulk capacitance charging. In dual-role ports it is used to disable the bulk capacitance when operating as a consumer.</p> <p>Note: This function is only available in specific device configurations.</p>
System Fault Detect	IFault	IS	<p>This active high signal is used by the power supplying device to notify when a system fault condition has occurred. This input is typically used for an over-current or over-voltage condition, but can be used for any system related failure. An external comparator should be used to filter any external noise on this input. The device firmware automatically handles all power exceptions by shutting down the power supply, re-enabling it, and restarting PD negotiation until successful.</p> <p>Note: The board design must ensure this signal is in a valid state by the time PD_EN_N asserts.</p>
System Reset	RESET_N	IS (PU)	System reset. This signal is active low.
Test	TEST	IS	Test signal. This signal is used for internal purposes only and must be connected to ground through a 1 K resistor for normal operation.

TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
No Connect	NC	-	No connect. For proper operation, this signal must not be connected.
SPI ROM Interface			
SPI ROM Clock	SPI_ROM_CLK	O8	SPI clock output to the serial ROM
SPI ROM Chip Enable	SPI_ROM_CE_N	O8	This is the active low SPI ROM chip enable output. If the SPI ROM interface is enabled, this signal should be pulled up to the SPI ROM Vcc rail.
SPI ROM Data In	SPI_ROM_DI	IS	SPI ROM data in
SPI ROM Data Out	SPI_ROM_DO	O8 (PD)	SPI ROM data out Note: This signal must be pulled-up to VDDIO with an external 10 kΩ resistor for proper operation.
Power/Ground			
VTR Supply Input	VTR	P	+3.3 to +5.0 V main power supply input. This signal must be connected to a 2.2 μF capacitor to ground. Refer to Figure 2-4 for additional power connection information.
+3.3 to +5.0 V Variable Voltage I/O Power	VDDIO	P	+3.3 V to +5.0 V variable I/O power supply input. Refer to Figure 2-4 for additional power connection information. Note: When using internal +3.3 V regulator, these pins must be externally connected to VDD33_CAP .
+5.0 V VBUS Input	VBUS	P	Optional +5.0 V auxiliary power input for the integrated power switch. This signal must be connected to ground or to a +5.0 V voltage source with a 2.2 μF capacitor to ground. Refer to Figure 2-4 for additional power connection information. Note: For externally powered devices (AC/DC adapters, charging adapters, etc.) this power pin is typically connected to ground. Note: This function is only available in specific device configurations.
+1.8V Power Delivery	PD_VDD18	P	+1.8 V power for Power Delivery PHY. Refer to Figure 2-4 for additional power connection information. Note: This pin must be connected to VDD18_CAP pin externally when using the internal VDD18 regulator.
+1.8 V Power Capacitance	VDD18_CAP	P	This pin is used to provide capacitance for the integrated +1.8 V regulator and must be connected to a 1 μF (<100 mΩ ESR) capacitor to ground. Refer to Figure 2-4 for additional power connection information.

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TABLE 2-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.8 V Analog Power Capacitance	VDD18A_CAP	P	This pin is used to provide capacitance for the integrated +1.8 V analog regulator and must be connected to a 1 μ F (<100 m Ω ESR) capacitor to ground. Refer to Figure 2-4 for additional power connection information.
+3.3 V Power Capacitance	VDD33_CAP	P	+3.3 V regulator output. This pin must be connected to a 1 μ F (<100 m Ω ESR) capacitor to ground. Refer to Figure 2-4 for additional power connection information.
Integrated Power Switch Capacitance	VSW_CAP	P	This pin is used to provide capacitance for the integrated power switch and must be connected to a 1 μ F (<100 m Ω ESR) capacitor to ground. Refer to Figure 2-4 for additional power connection information. Note: This function is only available in specific device configurations.
Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

2.3 Buffer Types

TABLE 2-3: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
PU	50 μ A (typical) internal pull-up. Unless otherwise noted in the signal description, internal pull-ups are always enabled. Note: Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 μ A (typical) internal pull-down. Unless otherwise noted in the signal description, internal pull-downs are always enabled. Note: Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
P	Power pin

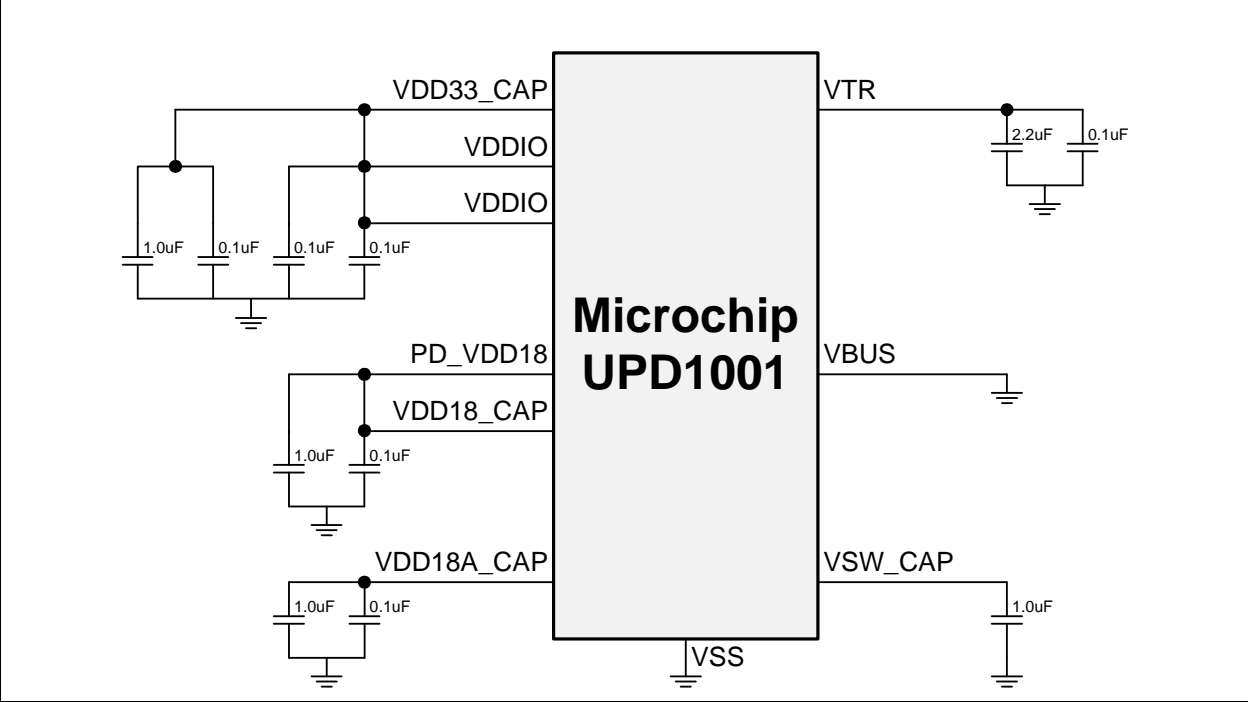
Note: All signals are 5 V tolerant.

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2.4 Power Connection Diagram

Figure 2-4 details the various power connection requirements.

FIGURE 2-4: POWER CONNECTION DIAGRAM



3.0 FUNCTIONAL DESCRIPTIONS

This chapter provides functional descriptions for the various device sub-systems:

- [Resets](#)
- [Power Management](#)
- [Configuration Selection \(CFG_SEL0/CFG_SEL1\)](#)
- [Voltage/Current Monitors \(VMON/IMON\)](#)
- [SPI ROM Controller](#)

3.1 Resets

The device includes the following reset controls:

- Power-On Reset (POR)
- External Chip Reset (**RESET_N**)

A system reset event via the external **RESET_N** pin or POR causes the following:

- All registers are set to their default values
- Pins are placed into their default state

The rising and falling Power-On Reset thresholds for each power supply are detailed in [Table 3-1](#).

TABLE 3-1: POR THRESHOLDS

POR	Rising Threshold	Falling Threshold
VDDIO Supply	2.7 V	2.35 V
VTR Supply	2.85 V	2.7 V

After power up, the POR initially de-asserts after the Rising Threshold is passed. In the event that the supply drops below the Falling Threshold, the POR will assert. The POR stays asserted until the Rising Threshold is once again crossed.

3.2 Power Management

The device will enter low power modes based on the state of the connection to the power delivery port partner. The low power connection states are defined for the device operating as a Provider (Provider/Consumer) or a Consumer (Consumer/Provider).

The device provides the following power states:

- Provider: [Wait Insert State](#)
- Consumer: [Sink Discovery State](#)

3.2.1 PROVIDER (OR PROVIDER/CONSUMER) POWER STATE

The device Provider configuration will enter a low power mode when it is not connected to a port partner and when a Standard-A plug is not inserted in the receptacle.

3.2.1.1 Wait Insert State

In the Wait Insert State, the device utilizes the insertion detect feature to enter a standby mode when waiting for a Standard-A plug to be inserted in the receptacle. On insertion of a Standard-A plug, the device will exit from the standby mode, initiate operation by enabling the supply output to 5Vsafe, and initiate the discovery of a port partner.

3.2.2 CONSUMER (OR CONSUMER/PROVIDER) POWER STATE

The device Consumer configuration enters a standby mode when it is not connected to a provider.

3.2.2.1 Sink Discovery State

In the Sink Discovery State, the device waits for the presence of VBUS to indicate a connection to provider. The device enters a standby state when waiting for the presence of VBUS. At the presence of VBUS, the Consumer exits the standby state and resumes full operation to establish a negotiated power contract with the Provider.

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3.3 Configuration Selection (CFG_SEL0/CFG_SEL1)

The UPD1001 provides a resistor/capacitor identification detection interface which is utilized to set various device configuration parameters via the Configuration Select pins:

- CFG_SEL0
- CFG_SEL1

Each Configuration Select pin can discriminate a number of quantized RC constants. The judicious selection of RC values provides a low cost means for system element configuration identification. The Configuration Select pins measure the charge/discharge time for the RC circuit connected to it (shown in Figure 3-1), providing the ability to differentiate 16 unique “bins” for each Configuration Select pin. The resistor and capacitor values for each Configuration Select bin are defined in Table 3-2.

FIGURE 3-1: CFG_SEL0/CFG_SEL1 RESISTOR-CAPACITOR CIRCUIT CONNECTIONS

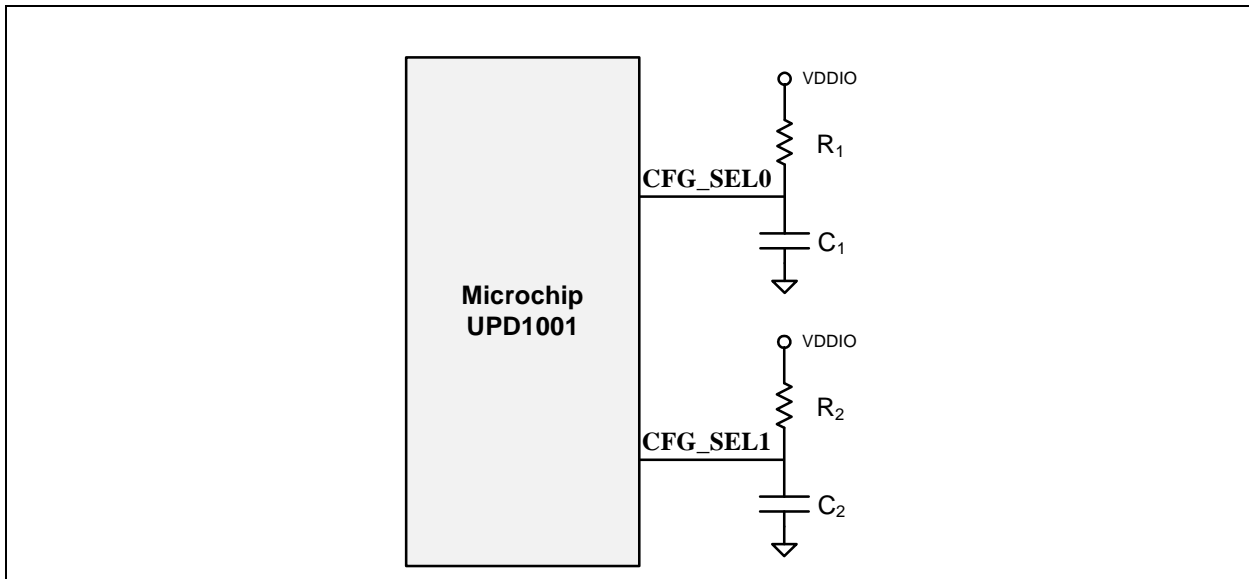


TABLE 3-2: CFG_SELX PIN RESISTOR-CAPACITOR BIN ALLOCATION

Bin	R _x (+/-1%)	C _x (+/-5%)
1	2.70 kΩ	None
2	2.70 kΩ	470 pF
3	4.87 kΩ	470 pF
4	8.66 kΩ	470 pF
5	15.40 kΩ	470 pF
6	2.70 kΩ	4.7 nF
7	4.87 kΩ	4.7 nF
8	8.66 kΩ	4.7 nF
9	15.40 kΩ	4.7 nF
10	2.70 kΩ	47.0 nF
11	4.87 kΩ	47.0 nF
12	8.66 kΩ	47.0 nF
13	15.40 kΩ	47.0 nF
14	2.70 kΩ	470 nF
15	4.87 kΩ	470 nF
16	8.66 kΩ	470 nF

Note: CFG_SEL0 and CFG_SEL1 bin definitions are identical.

By selecting specific bins on both the **CFG_SEL0** and **CFG_SEL1** pins, predefined configurations may be selected. These assignments configure multiple parameters of the device, including the following:

- [Pin Configuration](#)
- [Receptacle Type](#)
- [USB Power Delivery Role Selection](#)

A list of the configuration assignments along with the corresponding **CFG_SEL0** and **CFG_SEL1** bin settings, are detailed in the following section:

- [Section 3.3.1, "32-SQFN CFG_SELx Configuration Assignments," on page 21](#)

For details on each configurable parameter, refer to the following sub-sections.

Captive A cable to micro-B solutions are not listed in the **CFG_SELx** assignment tables, but can be addressed as follows:

- When **PD_DETECT** and **INSERTION_DETECT** pin are grounded, the device infers a PD cable is always attached and the source capabilities are limited to 3A.
- The **CFG_SELx** pin combinations for regular Standard-A solutions can be used for equivalent capabilities.

Captive B cable to A solutions are not listed in the **CFG_SELx** assignment tables, but can be addressed as follows:

- The proper capacitor marker, as per the *USB Power Delivery Specification*, should be positioned on the **PD_ID** pin to signal a 3A or 5A cable.
- The **CFG_SELx** pin combinations for regular Standard-B solutions can be used for equivalent capabilities.

Note: Only the bin combinations defined in the following tables are valid. All other bin combinations are reserved and must not be used.

3.3.1 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS

[Table 3-3](#) details the various 32-SQFN **CFG_SELx** configuration assignments.

TABLE 3-3: 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS

Config. #	32-SQFN Pin Config.	Receptacle Type	PD Consumer Abilities	PD Provider Abilities	VSEL0_N	VSEL1_N	VSEL2_N	VSEL3_N	CFG_SEL1 Bin	CFG_SEL0 Bin
1	32-A	STD-A	None	Profile 1	5	-	-	-	1	1
2	32-A	STD-A	None	Profile 1, 5V@3A	5	-	-	-	1	2
3	32-A	STD-A	None	Profile 1, 5V@5A	5	-	-	-	1	3
4	32-A	STD-A	None	Profile 1, 9V@2A	5	9	-	-	1	4
5	32-A	STD-A	None	Profile 1, 20V@3A	5	20	-	-	1	5
6	32-A	STD-A	None	Profile 1, 20V@5A	5	20	-	-	1	6
7	32-A	STD-A	None	Profile 2	5	12	-	-	1	7
8	32-A	STD-A	None	Profile 2, 9V@2A	5	9	12	-	1	8
9	32-A	STD-A	None	Profile 3	5	12	-	-	1	9
10	32-A	STD-A	None	Profile 3, 5V@3A	5	12	-	-	1	10
11	32-A	STD-A	None	Profile 3, 9V@3A	5	9	12	-	1	11
12	32-A	STD-A	None	Profile 3, 5V@3A, 9V@3A	5	9	12	-	1	12
13	32-A	STD-A	None	Profile 3, 5V@3A, 9V@3A, 16V@3A	5	9	12	16	1	13
14	32-A	STD-A	None	Profile 3, 9V@3A, PP-200	5	9	12	-	1	14
15	32-A	STD-A	None	Profile 3, PP-200	5	12	-	-	1	15
16	32-A	STD-A	None	Profile 4	5	12	20	-	1	16
17	32-A	STD-A	None	Profile 4, 5V@3A	5	12	20	-	2	1
18	32-A	STD-A	None	Profile 4, 9V@3A	5	9	12	20	2	2

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TABLE 3-3: 32-SQFN CFG_SELX CONFIGURATION ASSIGNMENTS (CONTINUED)

Config. #	32-SQFN Pin Config.	Receptacle Type	PD Consumer Abilities	PD Provider Abilities	VSEL0_N	VSEL1_N	VSEL2_N	VSEL3_N	CFG_SEL1 Bin	CFG_SEL0 Bin
19	32-A	STD-A	None	Profile 4, 5V@3A, 9V@3A	5	9	12	20	2	3
20	32-A	STD-A	None	Profile 4, 5V@3A, 16V@3A	5	12	16	20	2	4
21	32-A	STD-A	None	Profile 4, 9V@3A, PP-200	5	9	12	20	2	5
22	32-A	STD-A	None	Profile 4, 9V@5A, PP-200	5	9	12	20	2	6
23	32-A	STD-A	None	Profile 4, PP-200	5	12	20	-	2	7
24	32-A	STD-A	None	Profile 5	5	12	20	-	2	8
25	32-A	STD-A	None	Profile 5, 5V@5A	5	12	20	-	2	9
26	32-A	STD-A	None	Profile 5, 5V@5A, 16V@5A	5	12	16	20	2	10
27	32-A	STD-A	None	Profile 5, 5V@5A, 9V@5A	5	9	12	20	2	11
28	32-A	STD-A	None	Profile 5, PP-200	5	12	20	-	2	12
29	32-A	STD-A	None	Profile VSafe5V-L, 20V@3A	5	20	-	-	2	13
30	32-A	STD-A	None	Profile VSafe5V-L, 20V@5A	5	20	-	-	2	14
31	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1	5	-	-	-	2	15
32	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1, 5V@3A	5	-	-	-	2	16
33	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1, 5V@5A	5	-	-	-	3	1
34	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1, 9V@2A	5	9	-	-	3	2
35	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1, 20V@3A	5	20	-	-	3	3
36	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 1, 20V@5A	5	20	-	-	3	4
37	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 2	5	12	-	-	3	5
38	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 2, 9V@2A	5	9	12	-	3	6
39	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 3	5	12	-	-	3	7
40	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 3, 5V@3A	5	12	-	-	3	8
41	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 3, 5V@3A, 9V@3A	5	9	12	-	3	9
42	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 3, 5V@3A, 9V@3A, 16V@3A	5	9	12	16	3	10
43	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 4	5	12	20	-	3	11
44	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 4, 5V@3A	5	12	20	-	3	12
45	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 4, 5V@3A, 16V@3A	5	12	16	20	3	13
46	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 4, 5V@3A, 9V@3A	5	9	12	20	3	14
47	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 4, PP-200	5	12	20	-	3	15
48	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 5	5	12	20	-	3	16
49	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 5, 5V@5A	5	12	20	-	4	1
50	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 5, 5V@5A, 16V@5A	5	12	16	20	4	2
51	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 5, 5V@5A, 9V@5A	5	9	12	20	4	3
52	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile 5, PP-200	5	12	20	-	4	4
53	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile VSafe5V-L, 20V@3A	5	20	-	-	4	5
54	32-B	STD-B	NA (Profile VSafe5V-NC)	Profile VSafe5V-L, 20V@5A	5	20	-	-	4	6

3.3.2 PIN CONFIGURATION

The UPD1001 32-SQFN package provides selectable pin configurations via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in [Table 3-3, "32-SQFN CFG_SELx Configuration Assignments"](#). [Table 1-1, "UPD1001 Package/Pin Configuration Summary"](#) provides a summary of the available pin configurations. Refer to [Section 2.1, "32-Pin SQFN \(32-SQFN\)"](#) for details on the corresponding package pin definitions.

3.3.3 RECEPTACLE TYPE

The USB receptacle type is configurable between Standard-A and Standard-B types via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in [Table 3-3](#). Each of these receptacle type settings is detailed below.

3.3.3.1 Standard-A (STD-A)

The Standard-A setting informs the device that the designer is utilizing a Standard-A USB PD receptacle.

3.3.3.2 Standard-B (STD-B)

The Standard-B setting informs the device that the designer is utilizing a Standard-B USB PD receptacle.

3.3.4 USB POWER DELIVERY ROLE SELECTION

Depending on the receptacle type selected, the device may support and swap Consumer and Provider roles.

Standard-A receptacle (captive cable or otherwise) AC adapters only support the Provider role, and therefore do not support role swap. Standard-B receptacle AC adapters are Consumer/Providers that start operation in their default role of Consumer and support role swapping.

Swapping rules for Standard-B AC adapters are defined as follows:

- When operating as a Consumer:
 - Upon starting up, the AC adapter automatically initiates a swap request to its partner to become a Provider. If the partner rejects the request, the AC adapter will remain in its Consumer role until the partner requests a swap.
 - If the AC adapter receives a swap request from its partner to become a Consumer, it automatically accepts it.
- When operating as a Provider
 - The AC adapter will never initiate a swap request to its partner to become a Consumer.
 - If the AC adapter receives a swap request from its partner to become a Consumer, it automatically accepts it and will remain in the Consumer role (until the partner requests another swap back to Provider, or there is a hard reset or other exception condition that causes the protocol to be re-initiated from startup). The reason for this behavior is that the partner may have its own other external power which it decided to use instead of the AC adapter.

Note 1: All AC Adapters will only operate when connected to external AC power. An AC Adapter that is not plugged to the wall power supply will not be powered from its partner and will therefore not operate at all.

2: Standard-B receptacle AC adapters also support dead battery detection and can perform dead battery implicit swaps as per the PD specification.

The various Power Delivery Provider and Consumer capabilities are detailed in the following sub-sections.

3.3.4.1 Power Delivery Provider Capabilities

The USB PD Provider capabilities may be selected via the **CFG_SEL0** and **CFG_SEL1** pins, as defined in [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)"](#). Each of the PD Provider capabilities are detailed below. When capabilities are combined, it is possible that a device can support two or more currents for the same voltage. In this case, the device will only advertise one voltage with the highest current.

For example, a device that specifies support for "Profile 2 + 5V@3A" must support 5V@2A, 12V@1.5A and 5V@ 3A. In this case, the device will advertise only two Power Data Objects (PDO): 5V@3A and 12V@1.5A. The device will not explicitly advertise 5V@2A. However, a consumer that requires 5V@2A will request the 5V@ 3A PDO but only consume 2A.

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VSafe5V-L (5V@1A)

The Provider Capability Profile for VSafe5V Legacy (5V@1A) indicates that the UPD1001 supports providing 5 V at 1 A. This is typically used in dual-role ports that offer no real capability at 5 V (e.g., a Standard-B Consumer-Provider AC adapter port that only supports 20 V), but need to abide by the *USB Power Delivery Specification* requirement that at least one VSafe5V PDO be offered. Therefore, the capabilities of a legacy USB port (max 900 mA for USB 3.0) are included.

Profile 1

The Provider Capability Profile 1 indicates that the UPD1001 supports providing the voltages and currents needed to satisfy the USB PD profile 1, as defined by the *USB Power Delivery Specification* (5V@2A).

Profile 2

The Provider Capability Profile 2 indicates that the UPD1001 supports providing the voltages and currents needed to satisfy the USB PD profile 2, as defined by the *USB Power Delivery Specification* (5V@2A and 12V@1.5A).

Profile 3

The Provider Capability Profile 3 indicates that the UPD1001 supports providing the voltages and currents needed to satisfy the USB PD profile 3, as defined by the *USB Power Delivery Specification* (5V@2A and 12V@3A).

Profile 4

The Provider Capability Profile 4 indicates that the UPD1001 supports providing the voltages and currents needed to satisfy the USB PD profile 4, as defined by the *USB Power Delivery Specification* (5V@2A, 12V@3A, and 20V@3A).

Profile 5

The Provider Capability Profile 5 indicates that the UPD1001 supports providing the voltages and currents needed to satisfy the USB PD profile 5, as defined by the *USB Power Delivery Specification* (5V@2A, 12V@5A, and 20V@5A).

5V@3A

The Provider Capability 5V@3A indicates that the UPD1001 supports providing 5 V at 3 A. This option can be combined with other provider capability options.

5V@5A

The Provider Capability 5V@5A indicates that the UPD1001 supports providing 5 V at 5 A. This option can be combined with other provider capability options.

9V@2A

The Provider Capability 9V@2A indicates that the UPD1001 supports providing 9 V at 2 A. This option can be combined with other provider capability options.

9V@3A

The Provider Capability 9V@3A indicates that the UPD1001 supports providing 9 V at 3 A. This option can be combined with other provider capability options.

9V@5A

The Provider Capability 9V@5A indicates that the UPD1001 supports providing 9 V at 5 A. This option can be combined with other provider capability options.

16V@3A

The Provider Capability 16V@3A indicates that the UPD1001 supports providing 16 V at 3 A. This option can be combined with other provider capability options.

16V@5A

The Provider Capability 16V@5A indicates that the UPD1001 supports providing 16 V at 5 A. This option can be combined with other provider capability options.

20V@3A

The Provider Capability 20V@3A indicates that the UPD1001 supports providing 20 V at 3 A. This option can be combined with other provider capability options.

20V@5A

The Provider Capability 20V@5A indicates that the UPD1001 supports providing 20 V at 5 A. This option can be combined with other provider capability options.

Peak Power-Capable Setting 0b11 - 200% (PP-200)

The Peak Power-Capable 200% indicates that the UPD1001 supports providing 200% of the current limit for a 1 ms time duration at 5% duty cycle. This will add the correct 0b11 bits to the PDO.

3.3.4.2 PD Consumer Capabilities

AC adapters are not intended to be Consumers. However, a need exists for Standard-B receptacle (Consumer/Provider) AC adapters for powering notebooks through their PD enabled Standard-A host ports. The Power Delivery Specification requires any consumer port to at least support VSafe5V, so a minimal non-consuming capability is defined (VSafe5V-NC).

The USB PD Consumer capabilities may be selected via the `CFG_SEL0` and `CFG_SEL1` pins, as defined in [Section 3.3, "Configuration Selection \(CFG_SEL0/CFG_SEL1\)"](#). Each of the PD Consumer capabilities are detailed below.

VSafe5V-NC (5V@0A)

The Consumer Capability Profile for VSafe5V Non-Consuming indicates to the UPD1001 that this solution must have only 5 V input sources and must not consume. This is typically used in dual-role ports that offer no capability in their default role (e.g., a Standard-B Consumer-Provider AC adapter port).

3.4 Voltage/Current Monitors (VMON/IMON)

3.4.1 VMON

The integrated voltage monitor utilizes the `VMON` pin to read a stepped down voltage representation of the VBUS voltage. This pin must be connected to a voltage divider circuit as specified in [Section 2.4, "Power Connection Diagram," on page 18](#). The device monitors the VBUS voltage as a provider to manage the behavior of the power supply, detecting power supply transitions and over/under-voltage conditions.

3.4.1.1 Power Supply Transitions

Using `VMON`, the device monitors the voltage on VBUS to manage the transitions of the supply output. The supply power-on and power-off transitions are determined to be at their final states when reaching predefined voltage thresholds, as detailed in [Table 3-4](#). The power-on threshold indicates when the supply has reached the defined voltage. The power-off threshold indicates when the supply output is discharged. All voltage transitions are bound by an internal timer. If the voltage transition times out, the `FAULT_N` pin will be asserted until the power transition is successfully completed.

TABLE 3-4: VMON POWER-ON/OFF TRANSITION THRESHOLDS

	Voltage Threshold (V)		
	Min.	Typical	Max
Power-On	-	3	-
Power-Off	-	2	-

3.4.1.2 Overvoltage Condition

Using `VMON`, the device monitors the voltage on VBUS to detect an overvoltage condition on the supply output. The overvoltage condition is determined when the predefined overvoltage threshold is crossed, as detailed in [Table 3-5](#).

On the occurrence of the overvoltage condition:

- The supply output will be turned off and discharged.
- The `FAULT_N` pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, `FAULT_N` will be strobed approximately every 5 seconds.

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TABLE 3-5: VMON OVERVOLTAGE THRESHOLDS

	Voltage Threshold (V)		
	Min.	Typical	Max
5 V	-	6.0	6.9
9 V	-	10.4	12.0
12 V	-	13.7	15.8
16 V	-	18.1	20.9
20 V	-	22.5	26.9

3.4.1.3 Undervoltage Condition

Using **VMON**, the device monitors the voltage on **VBUS** to detect an undervoltage condition on the supply output. The undervoltage condition is determined when the predefined undervoltage threshold is crossed, as detailed in [Table 3-6](#). On the occurrence of the undervoltage condition:

- The supply output will be turned off and discharged.
- The **FAULT_N** pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, **FAULT_N** will be strobed approximately every 5 seconds.

TABLE 3-6: VMON UNDERVOLTAGE THRESHOLDS

	Voltage Threshold (V)		
	Min.	Typical	Max
5 V	-	4.5	-
9 V	-	8.1	-
12 V	-	10.8	-
16 V	-	14.4	-
20 V	-	18.0	-

3.4.2 IMON

The integrated current monitor utilizes the **IMON** pin to read a voltage representation of the power supply output current. This pin should be fed by a current sense amplifier tuned to output 3.0 V when 6.0 A is flowing on **VBUS**. On connection of a port partner and the completion of a negotiated power contract, the overcurrent threshold is set based on the negotiated current. When the device is not connected to a port partner, the overcurrent threshold will be set to the default level. On the occurrence of an overcurrent condition:

- The supply output will be turned off and discharged.
- The **FAULT_N** pin will be strobed approximately every 500ms.
- If more than 3 consecutive exceptions occur within a 4 second period, **FAULT_N** will be strobed approximately every 5 seconds.

TABLE 3-7: IMON OVERCURRENT THRESHOLDS

Negotiated Profile Current	Overcurrent Threshold (A)		
	Min.	Typical	Max
1.5 A	-	1.73	1.95
2 A	-	2.30	2.60
3 A	-	3.45	3.90
5 A	-	5.75	6.50

Note: Only sourced currents (when the PD port is operating as a provider) can be monitored by **IMON**. If it is desired to monitor a sinking current (when the port is operating as a consumer), an external circuit should be used and the condition indicated to the device via the **IFault** pin.

3.5 SPI ROM Controller

The device is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

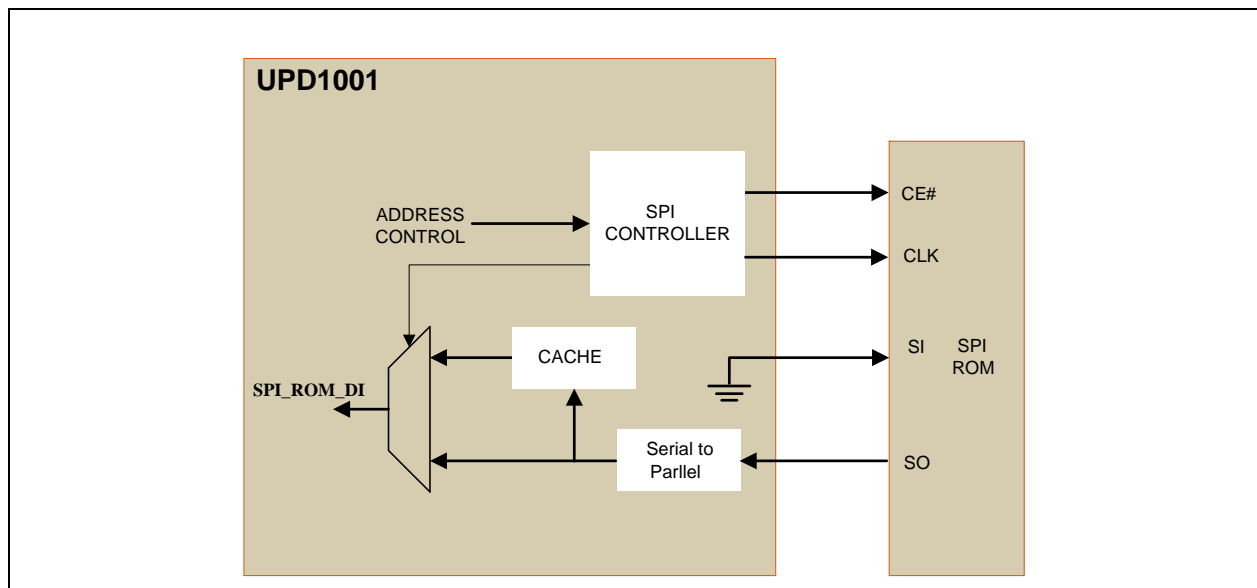
Note: Microchip suggests using the SST 25 series serial flash family, such as the SST25VF064C.

3.5.1 OPERATION OF THE HI-SPEED READ SEQUENCE

The SPI controller will automatically handle code reads going out to the SPI ROM Address. When the controller detects a read, the controller drops the **SPI_ROM_CE_N**, and puts out a 0x0B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next eight clocks clock in the first byte. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

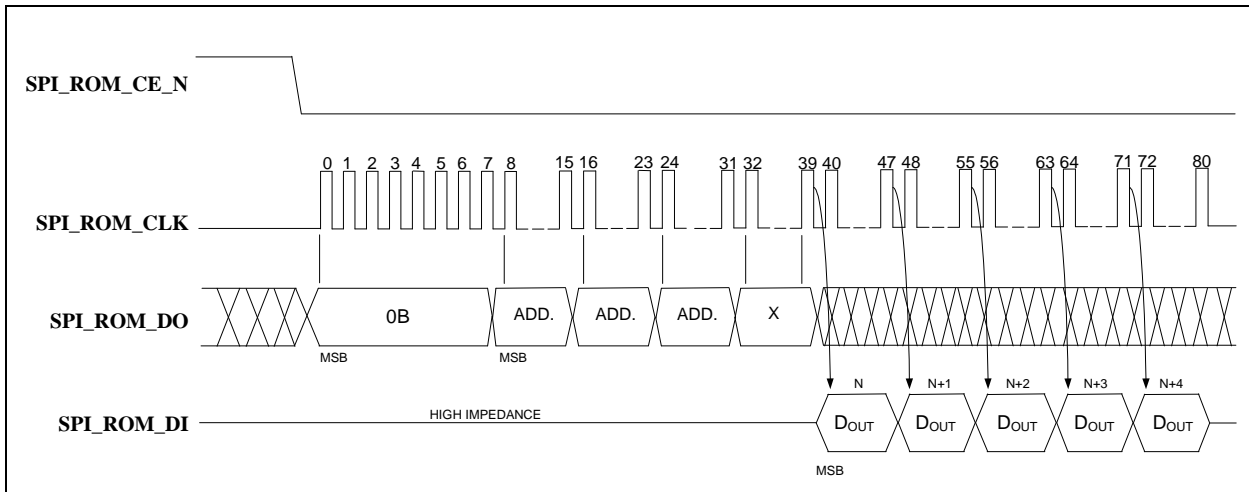
After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address is anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_ROM_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

FIGURE 3-2: SPI ROM HI-SPEED READ OPERATION



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FIGURE 3-3: SPI ROM HI-SPEED READ SEQUENCE



3.5.2 OPERATION OF THE DUAL HI-SPEED READ SEQUENCE

The SPI controller also supports dual data mode (at 30 MHz SPI speed only). When configured in dual mode, the SPI controller will automatically handle reads going out to the SPI ROM. When the controller detects a read, the controller drops the **SPI_ROM_CE_N**, and puts out a 0x3B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next four clocks clock in the first byte. The data appears two bits at a time on data out and data in. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, the address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address is anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_ROM_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

FIGURE 3-4: SPI ROM DUAL HI-SPEED READ OPERATION

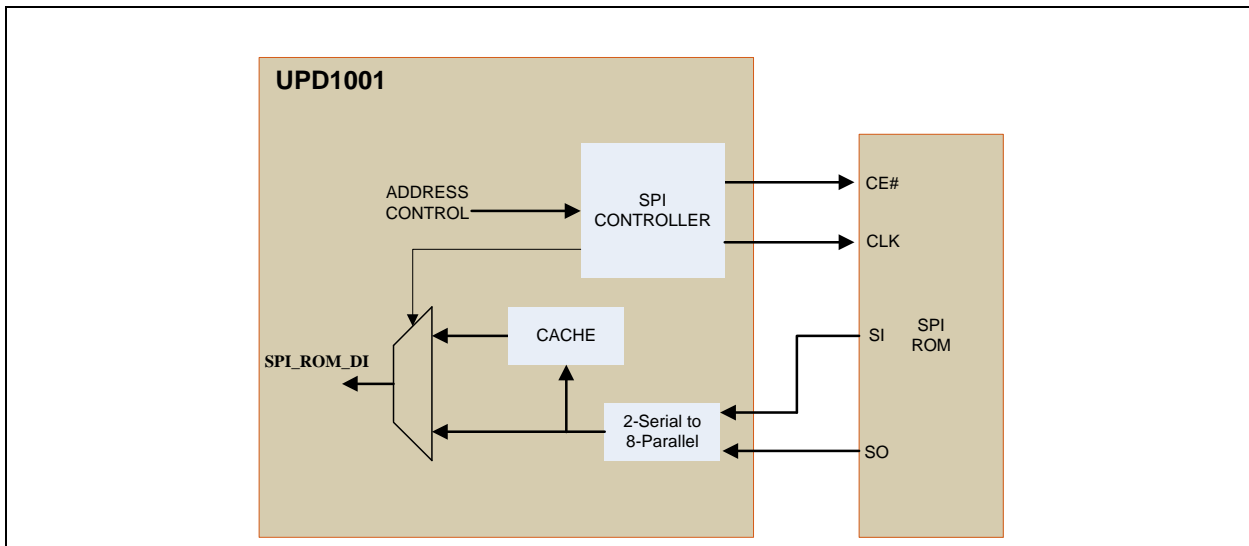
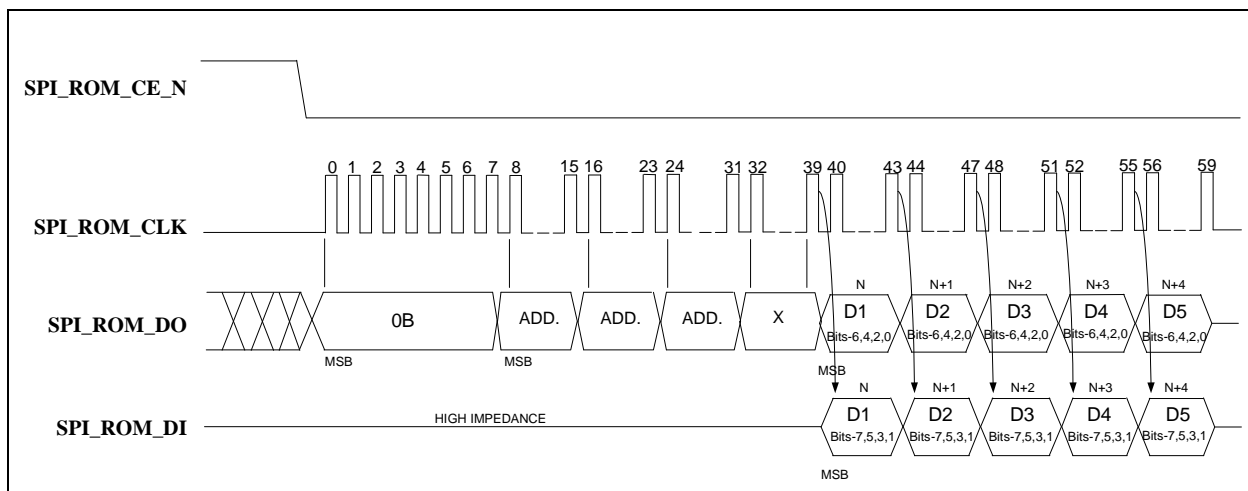


FIGURE 3-5: SPI ROM DUAL HI-SPEED READ SEQUENCE



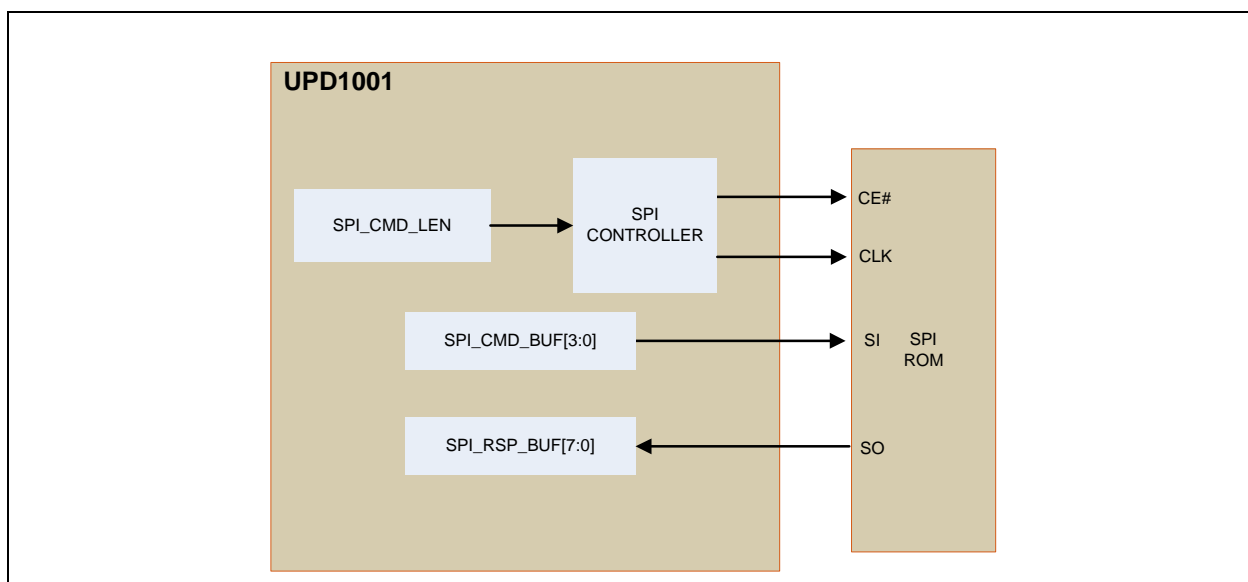
3.5.3 32-BYTE CACHE

There is a 32-byte pipeline cache, and associated with the cache is a base address pointer and a length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache, and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the device does a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

3.5.4 INTERFACE OPERATION TO SPI PORT WHEN NOT PERFORMING FAST READS

There is an 8-byte command buffer: `SPI_CMD_BUF[7:0]`; an 8-byte response buffer: `SPI_RESP_BUF[7:0]`; and a length register that counts out the number of bytes: `SPI_CMD_LEN`. Additionally, there is a self-clearing GO bit in the `SPI_CTL` Register. Once the GO bit is set, the device drops `SPI_ROM_CE_N`, and starts clocking. It will put out `SPI_CMD_LEN` X 8 number of clocks. After the first byte, the COMMAND, has been sent out, and the `SPI_ROM_DI` is stored in the `SPI_RESP` buffer. If the `SPI_CMD_LEN` is longer than the `SPI_CMD_BUF`, don't cares are sent out on the `SPI_ROM_DO` line. This mode is used for program execution out of internal RAM or ROM.

FIGURE 3-6: SPI ROM INTERNALLY-CONTROLLED OPERATION

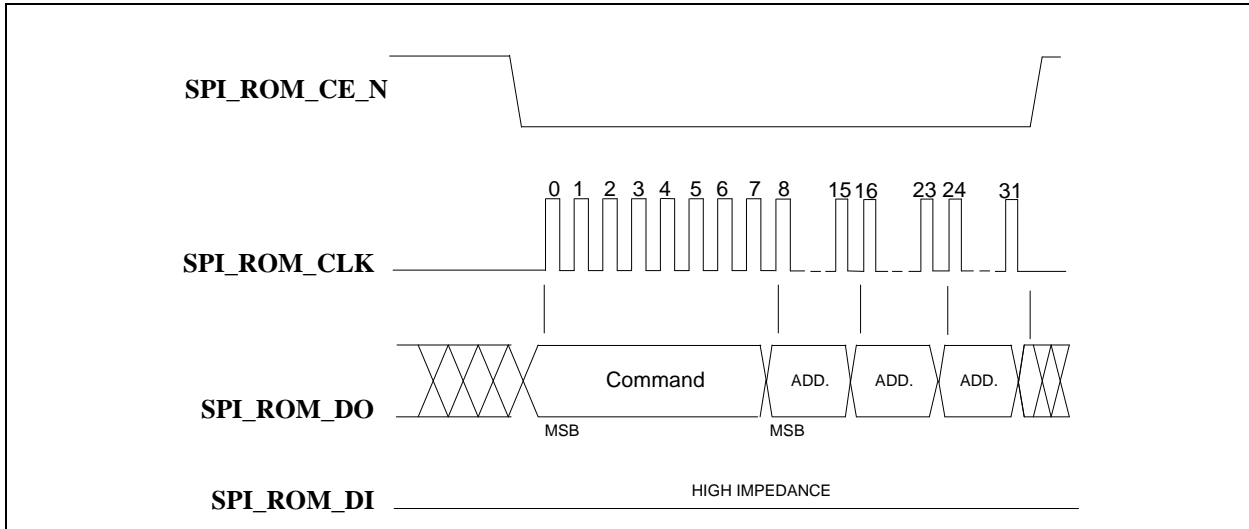


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3.5.4.1 Erase Example

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To do this, the device first drops **SPI_ROM_CE_N**, then counts out 8 clocks. It then puts out the 8 bits of command, followed by 24 bits of address of the location to be erased on the **SPI_ROM_DO** pin. When the transfer is complete, the **SPI_ROM_CE_N** goes high, while the **SPI_ROM_DI** line is ignored in this example.

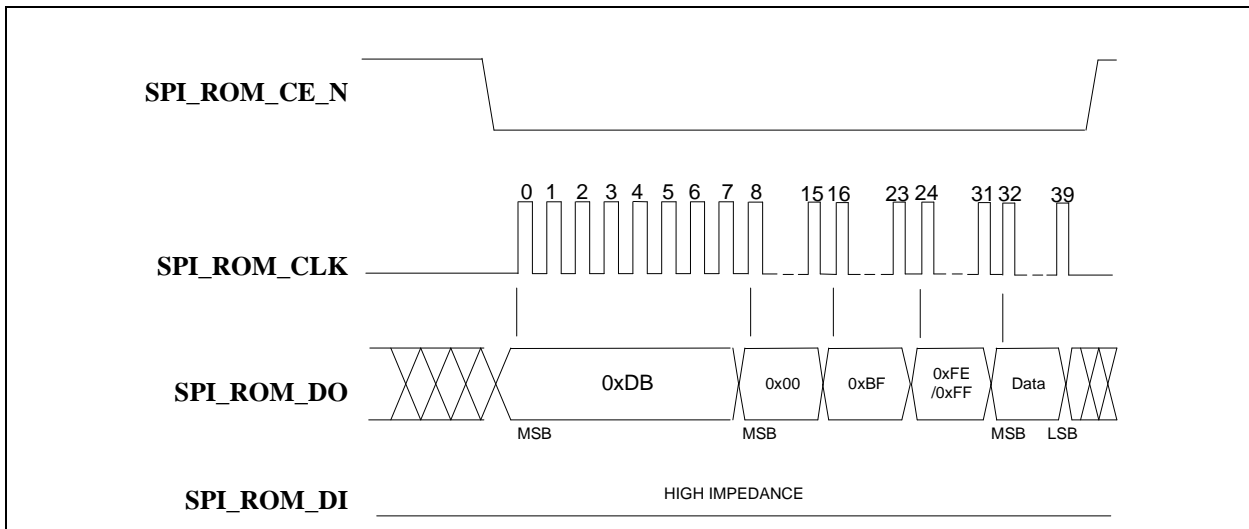
FIGURE 3-7: SPI ROM ERASE SEQUENCE



3.5.4.2 Byte Program Example

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drops **SPI_ROM_CE_N**, 8 bits of command are clocked out, followed by 24 bits of address, and one byte of data on the **SPI_ROM_DO** pin. The **SPI_ROM_DI** line is not used in this example.

FIGURE 3-8: SPI ROM BYTE PROGRAM



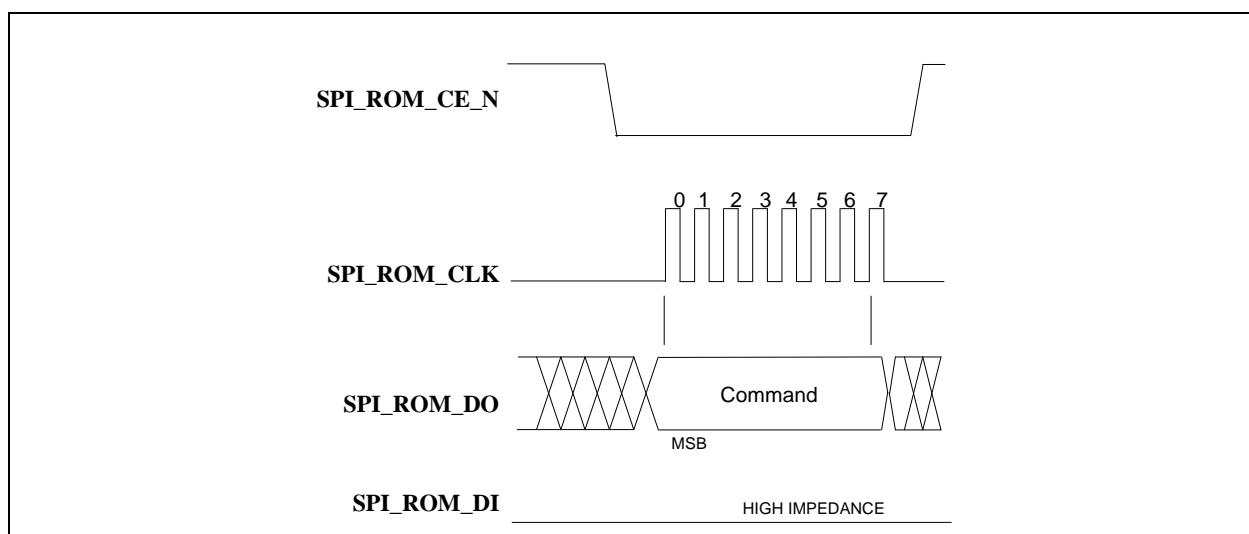
3.5.4.3 Command Only Program Example

To perform a single byte command such as the following:

- WRDI
- WREN
- EWSR
- CHIP_ERASE
- EBSY
- DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drops **SPI_ROM_CE_N**, then 8 bits of the command are clocked out on the **SPI_ROM_DO** pin. The **SPI_ROM_DI** is not used in this example.

FIGURE 3-9: SPI ROM COMMAND ONLY SEQUENCE

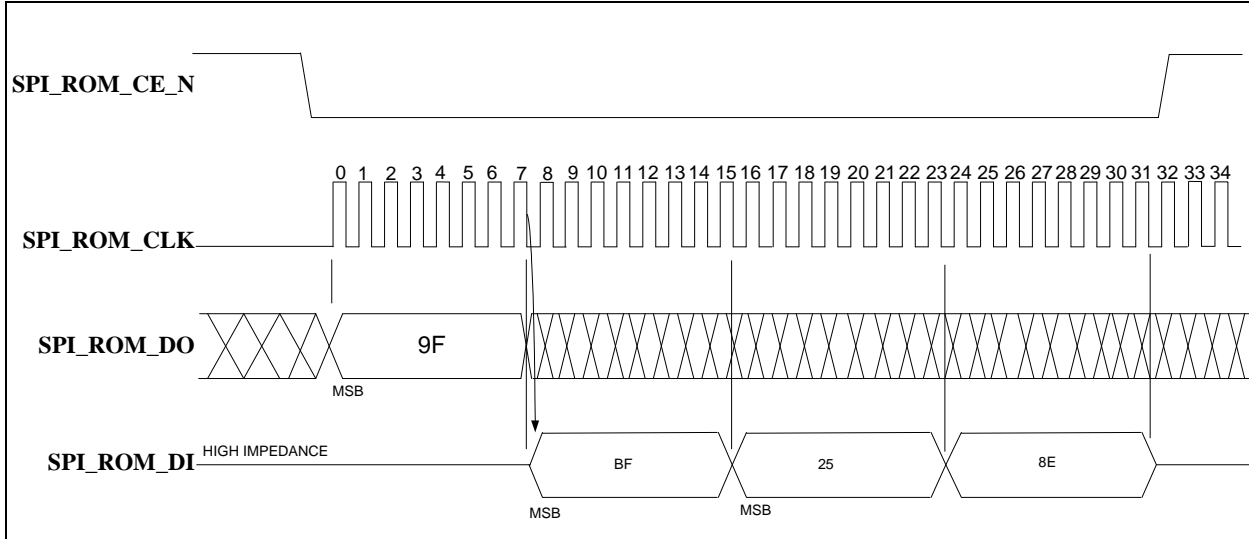


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3.5.4.4 JEDEC-ID Read Example

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF and the length of the transfer is 4 bytes. The device first drops **SPI_ROM_CE_N**, then 8 bits of the command are clocked out, followed by the 24 bits of dummy bytes (due to the length being set to 4) on the **SPI_ROM_DO** pin. When the transfer is complete, the **SPI_ROM_CE_N** goes high. After the first byte, the data on **SPI_ROM_DI** is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

FIGURE 3-10: SPI ROM JEDEC-ID SEQUENCE



4.0 OPERATIONAL CHARACTERISTICS

4.1 Absolute Maximum Ratings*

Supply Voltage (VDDIO, VTR) (Note 1)	0 V to +6.0 V
Positive voltage on input signal pins, with respect to ground	+6.0 V
Negative voltage on input signal pins, with respect to ground	-0.5 V
Storage Temperature	-55°C to +150°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020
HBM ESD Performance	+/-2 kV

Note 1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 4.2, "Operating Conditions**", Section 4.4, "DC Specifications", or any other applicable section of this specification is not implied.

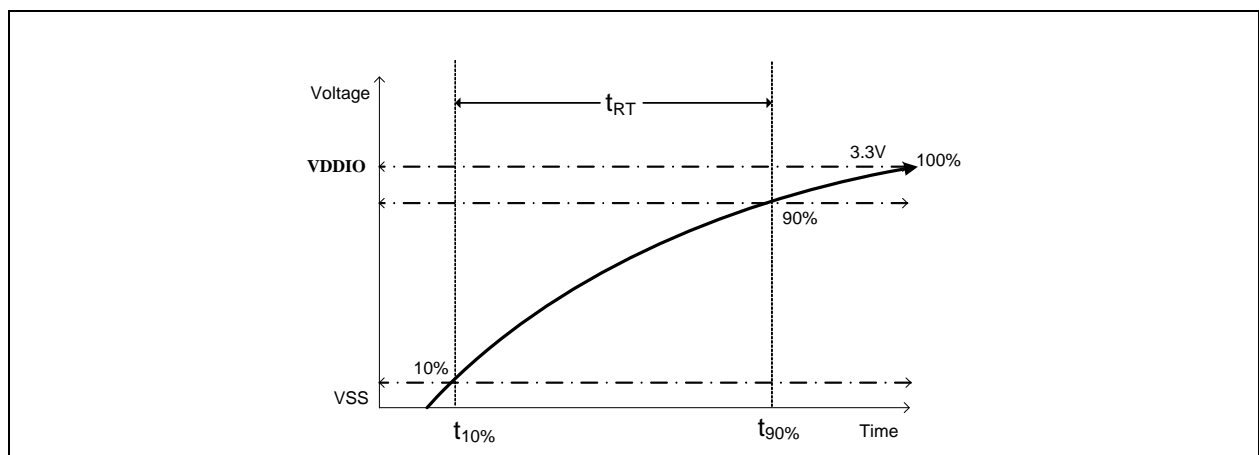
4.2 Operating Conditions**

Supply Voltage (VTR)	+3.1 V to +5.3 V
Supply Voltage (VDDIO)	+3.1 V to +3.47 V
Positive voltage on input signal pins, with respect to ground	+3.3 V
Negative voltage on input signal pins, with respect to ground	-0.3 V
Positive voltage on VMON and IMON pins, with respect to ground	VDDIO
Negative voltage on VMON and IMON pins, with respect to ground	-0.3 V
Power Supply Rise Time Max t_{RT} (Figure 4-1)	TBD
Ambient Operating Temperature in Still Air (T_A)	Note 2

Note2: 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

FIGURE 4-1: SUPPLY RISE TIME MODEL



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4.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

Note: Maximum values represent very short bursts of activity over a small amount of time. Typical values represent averaged current consumption over time.

TABLE 4-1: DEVICE POWER CONSUMPTION

Power State	VTR Supply Current		
	Typical	Max	Units
RESET	0.325	3.5	mA
PROVIDER MODE			
Wait Insert State	1.2	16.2	mA
Legacy Device Connected	14.6	58.5	mA
PD Device Connected	28.0	69.0	mA
CONSUMER MODE			
Sink Discovery State / Legacy Device Connected	10.0	45.0	mA
PD Device Connected	28.0	69.0	mA

4.4 DC Specifications

TABLE 4-2: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3		0.8	V	
High Input Level	V_{IHI}	2.5		VDDIO+0.3	V	
Negative-Going Threshold	V_{ILT}	1.25	1.35	1.55	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.40	1.65	1.76	V	Schmitt trigger
Schmitt Trigger Hysteresis ($V_{IHT} - V_{ILT}$)	V_{HYS}	188	225	250	mV	
Input Leakage ($V_{IN} = VSS$ or VDDIO)	I_{IH}	-9.79		7.14	nA	Note 3
Input Capacitance	C_{IN}			3	pF	
O8 Type Buffers						
Low Output Level	V_{OL}			0.35	V	$I_{OL} = -8$ mA
High Output Level	V_{OH}	VDDIO - 0.7			V	$I_{OH} = 8$ mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.35	V	$I_{OL} = -8$ mA

Note3: This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 μ A per-pin (typical).

4.5 AC Specifications

This section details the various AC timing specifications of the device.

4.5.1 RESET TIMING

Figure 4-2 illustrates the **RESET_N** timing requirements. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified.

Refer to Section 3.1, "Resets," on page 19 for additional information on resets.

FIGURE 4-2: RESET_N TIMING

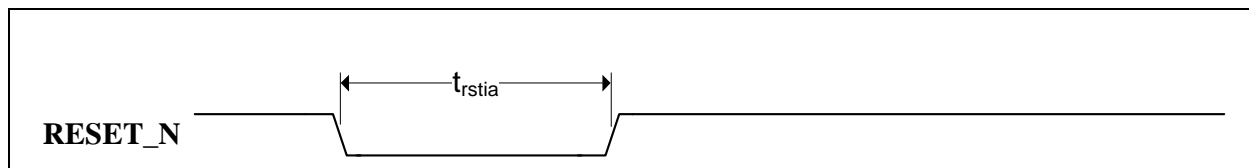


TABLE 4-3: RESET_N TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	RESET_N input assertion time	1			μs

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4.5.2 SPI ROM CONTROLLER TIMING

The following specifies the SPI ROM Controller timing requirements for the device.

FIGURE 4-3: SPI ROM CONTROLLER TIMING

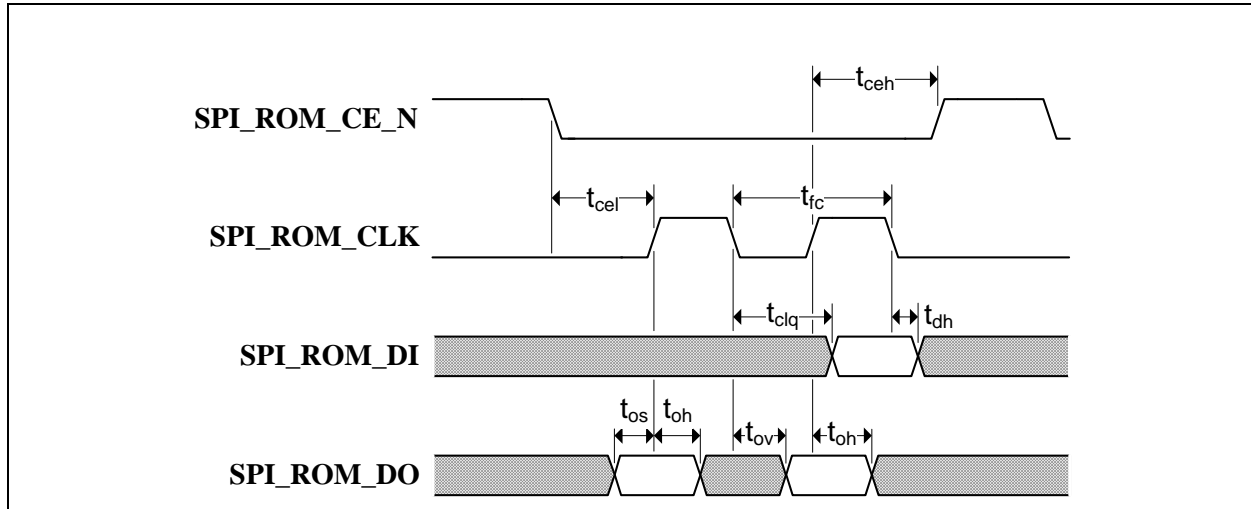


TABLE 4-4: SPI ROM CONTROLLER TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency	46.86	48	48.62	MHz
t_{ceh}	Chip enable (SPI_ROM_CE_EN) high time		50		ns
t_{clq}	Clock to input data		15		ns
t_{dh}	Input data hold time	0.70	3	4.52	ns
t_{os}	Output setup time	5.35	7	8.28	ns
t_{oh}	Output hold time	11.57	13	15.22	ns
t_{ov}	Clock to output valid	1.16	2	3.3	ns
t_{cel}	Chip enable (SPI_ROM_CE_EN) low to first clock		12		ns
t_{ceh}	Last clock to chip enable (SPI_ROM_CE_EN) high		12		ns

4.5.3 USB POWER DELIVERY SIGNAL TIMING

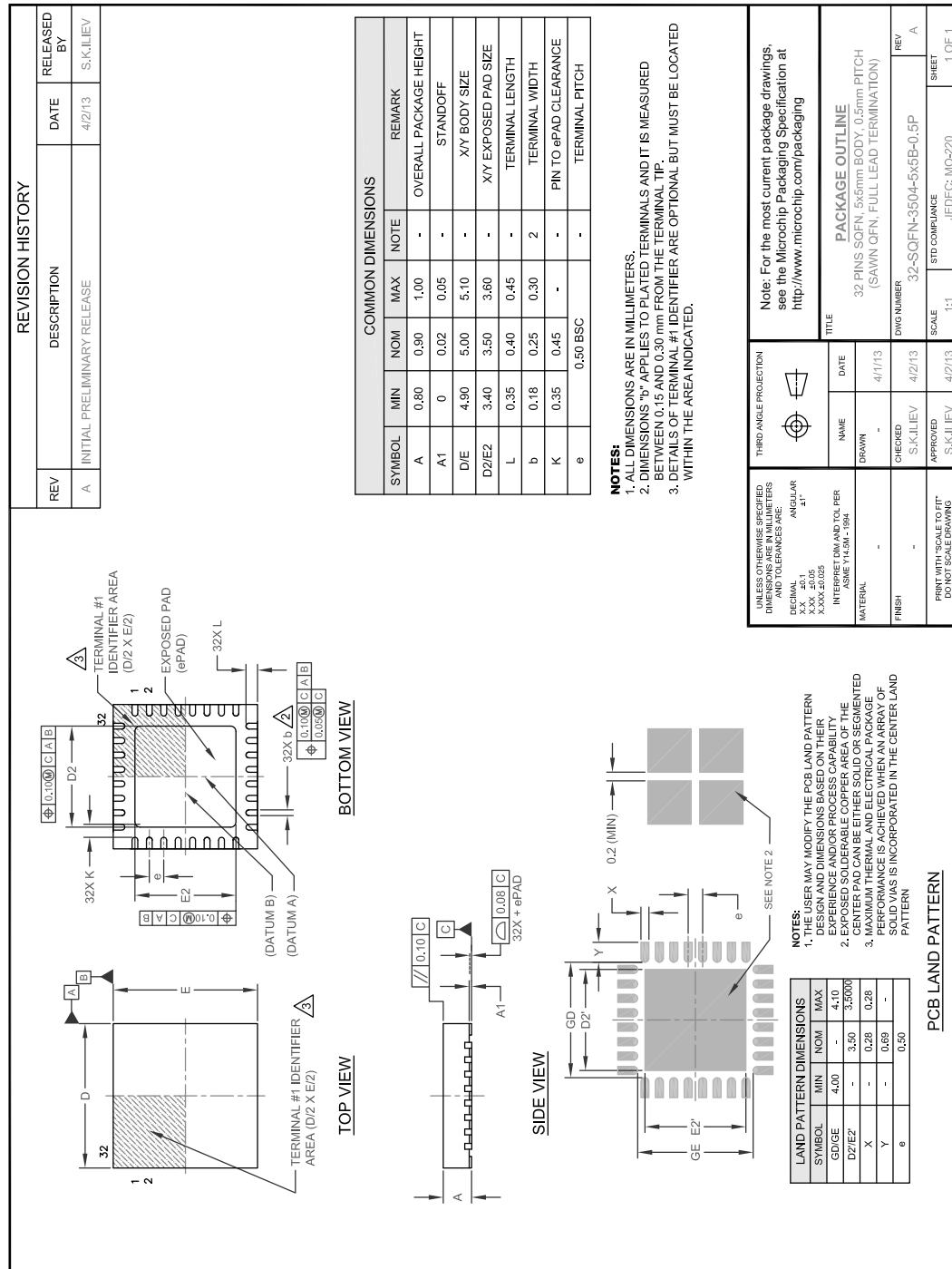
All USB Power Delivery signals (**PD_DATA**, **PD_ID**) conform to the voltage, power, and timing characteristics/specifications as set forth in the USB Power Delivery Specification. Please refer to the *USB Power Delivery Specification*, available at <http://www.usb.org>.

5.0 PACKAGE OUTLINE

5.1 32-SQFN

Note: For the most current package drawings, see the Microchip Packaging Specification at: <http://www.microchip.com/packaging>.

FIGURE 5-1: 32-SQFN PACKAGE



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6.0 REVISION HISTORY

TABLE 6-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001759B (12-02-14)	Table 3-4 , Table 3-5 , Table 3-6 , and Table 3-7	Added IMON/VMON thresholds (was TBD).
	Section 4.5 , "AC Specifications," on page 35	Removed "VMON/IMON FAULT RECOVERY TIMING" and "IFault RECOVERY TIMING" sections.
	Table 3-2 , "CFG_SELx PIN Resistor-Capacitor BIN ALLOCATION," on page 20	Updated Cx tolerance to +/-5%.
	Table 4-1 , "Device Power Consumption," on page 34	Updated power consumption table.
	All: Cover, Intro	Removed "Programmable" from part description.
	All: Cover, Intro, Pin Descriptions, Package Drawings, Ordering Codes	Removed 28-TSSOP package option.
DS00001759A		Initial Release

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PRODUCT IDENTIFICATION SYSTEM

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<u>PART NO.</u>	[X]	-	XX	/	XX
Device	Tape and Reel Option		Temperature Range		Package
Device:	UPD1001				
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel (Note 1)				
Temperature Range:	A = 0°C to +70°C (Commercial) AI = -40°C to +85°C (Industrial)				
Package:	MQ = 32-pin SQFN				

Examples:

- a) UPD1001-A/MQ
Tray, Commercial temp., 32-pin SQFN
- b) UPD1001T-AI/MQ
Tape & reel, Industrial temp., 32-pin SQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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