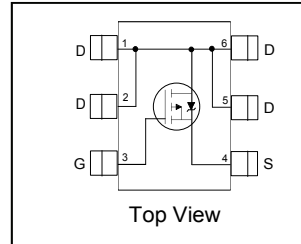


- Ultra Low On-Resistance
- P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Low Gate Charge
- Lead-Free
- Halogen-Free

HEXFET® Power MOSFET

$V_{DS}$	$R_{DS(on)}$ (max)	$I_D$
- 40V	<b>112mΩ @ <math>V_{GS} = -10V</math></b>	<b>-3.4A</b>
	<b>190mΩ @ <math>V_{GS} = -4.5V</math></b>	<b>-2.7A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

These P-channel HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

The TSOP-6 package with its customized lead frame produces a HEXFET® power MOSFET with  $R_{DS(on)}$  60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and  $R_{DS(on)}$  reduction enables a current-handling increase of nearly 300% compared to the SOT-23.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF5803PbF	TSOP-6	Tape and Reel	3000	IRF5803TRPbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	-40	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	- 3.4	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-2.7	
$I_{DM}$	Pulsed Drain Current ①	- 27	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation ③	2.0	W
$P_D @ T_A = 70^\circ C$	Maximum Power Dissipation ③	1.3	
	Linear Derating Factor	16	mW/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		


**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	62.5	°C/W

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

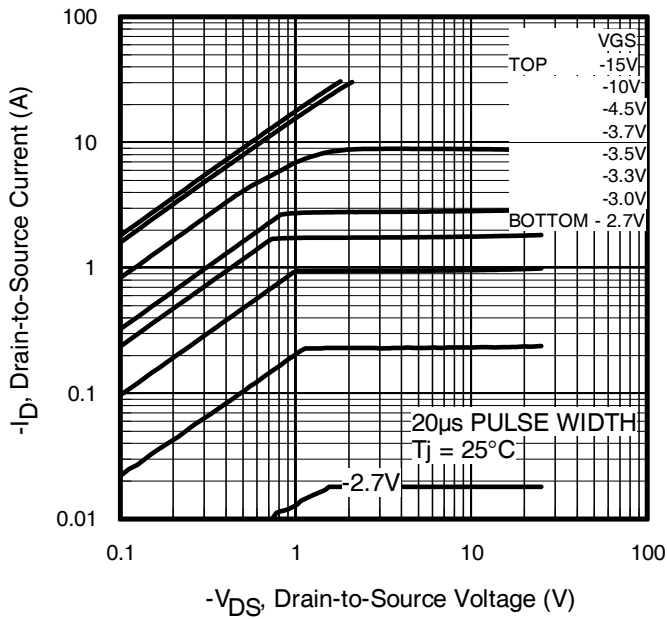
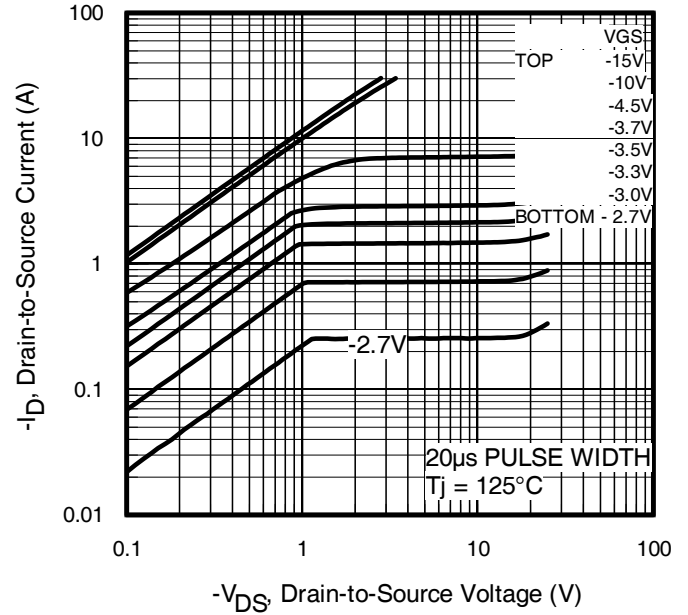
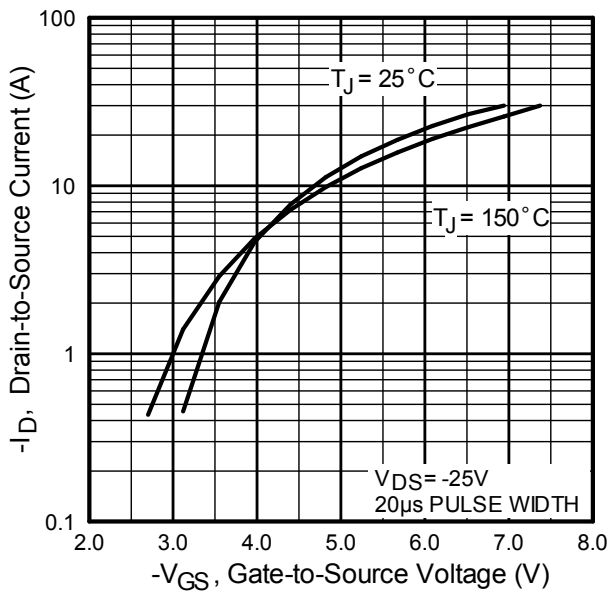
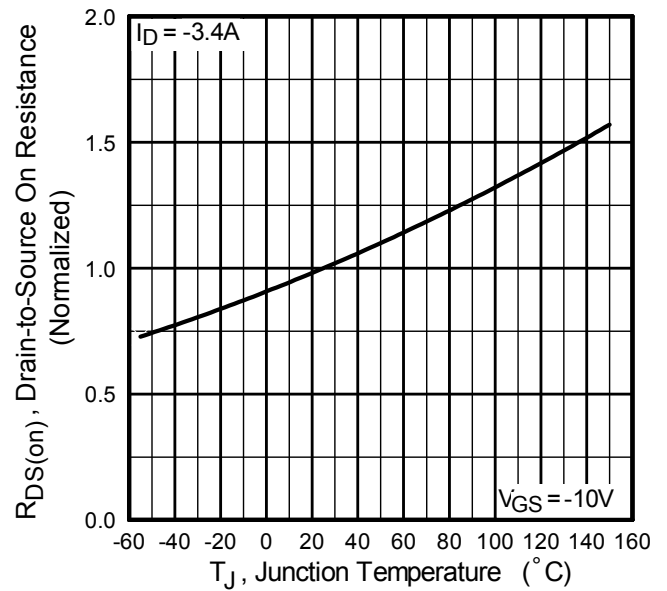
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.03	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	112	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -3.4A
		—	—	190		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.7A
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	—	-3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Trans conductance	4.0	—	—	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -3.4A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-10	μA	V <sub>DS</sub> = -32V, V <sub>GS</sub> = 0V
		—	—	-25		V <sub>DS</sub> = -32V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	25	37	nC	I <sub>D</sub> = -3.4A
Q <sub>gs</sub>	Gate-to-Source Charge	—	4.5	6.8		V <sub>DS</sub> = -20V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	3.5	5.3		V <sub>GS</sub> = -10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	43	—	ns	V <sub>DD</sub> = -20V <sup>②</sup>
t <sub>r</sub>	Rise Time	—	550	—		I <sub>D</sub> = -1.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	88	—		R <sub>G</sub> = 6.0Ω
t <sub>f</sub>	Fall Time	—	50	—		V <sub>GS</sub> = -10V
C <sub>iss</sub>	Input Capacitance	—	1110	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	93	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	73	—		f = 100KHz

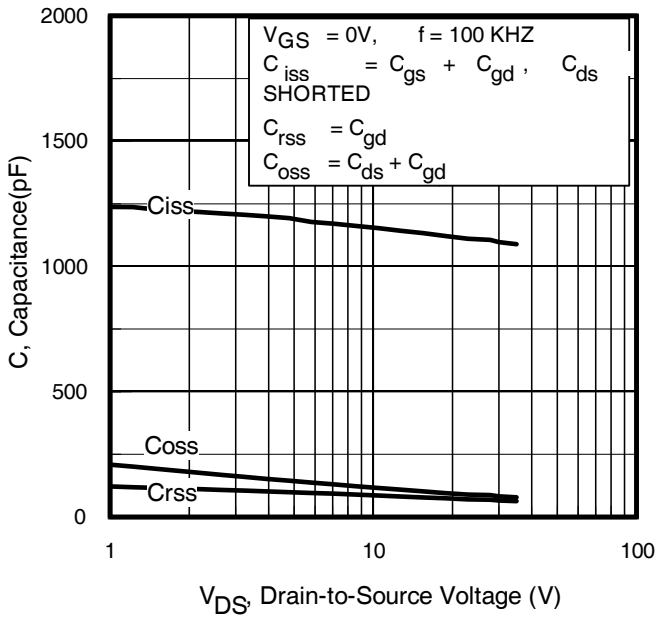
**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	-27		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -2.0A, V <sub>GS</sub> = 0V <sup>②</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	27	40	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -2.0A
Q <sub>rr</sub>	Reverse Recovery Charge	—	34	50	nC	di/dt = 100A/μs <sup>②</sup>

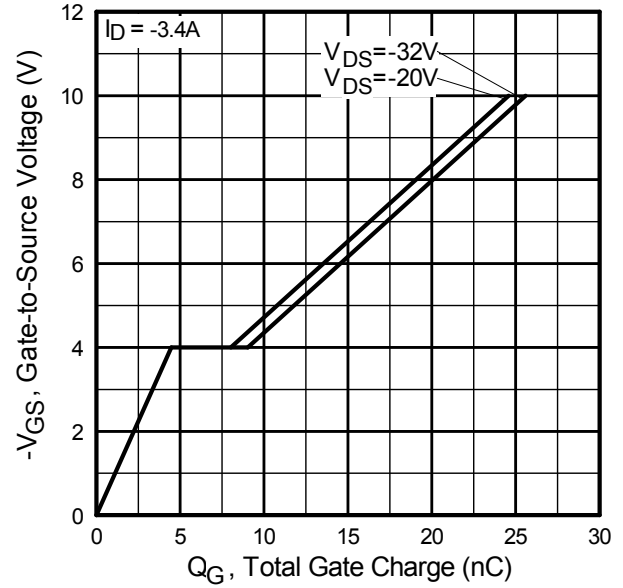
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ③ Surface mounted on 1 in square Cu board

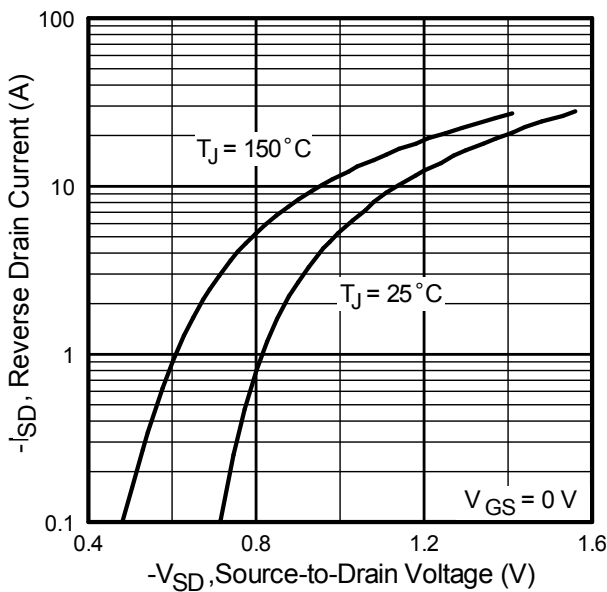

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature



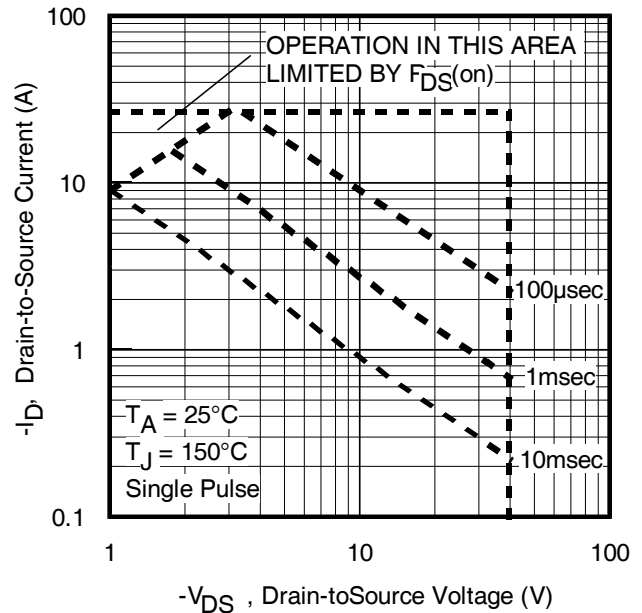
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



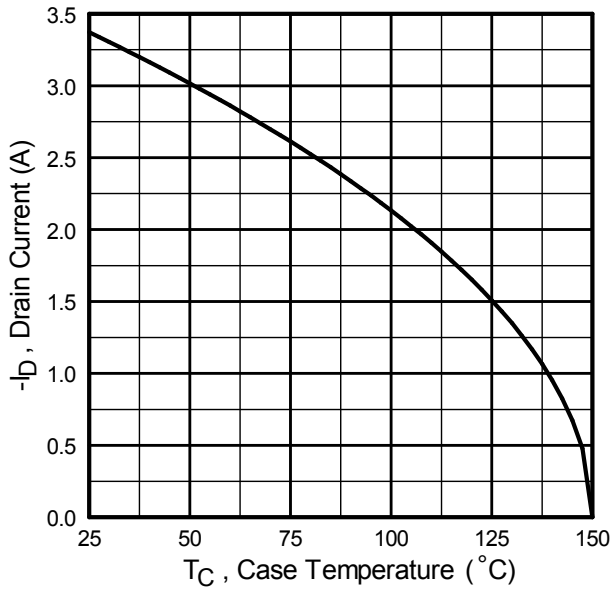
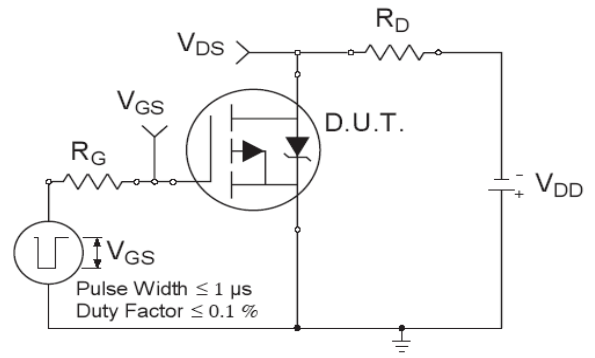
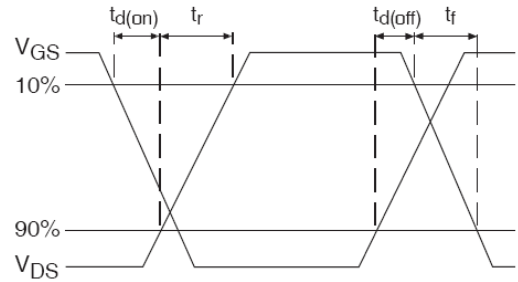
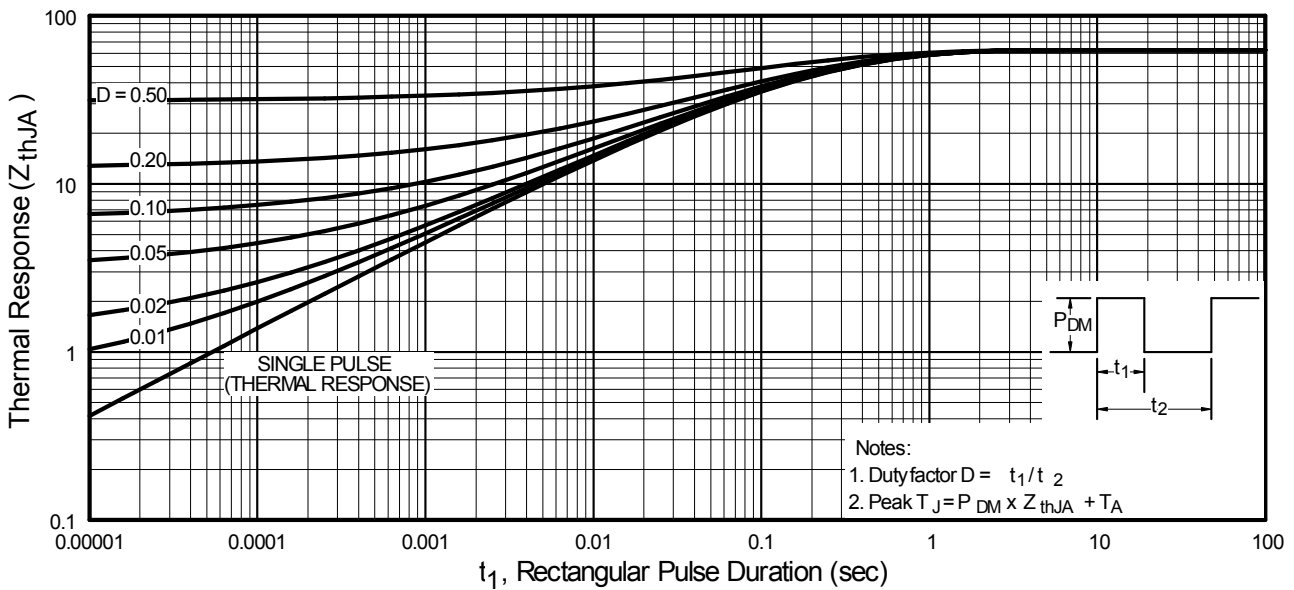
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

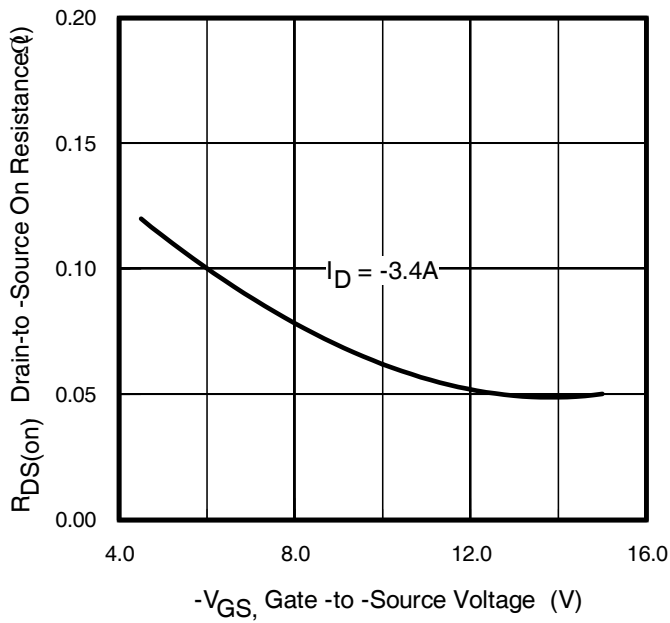


**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

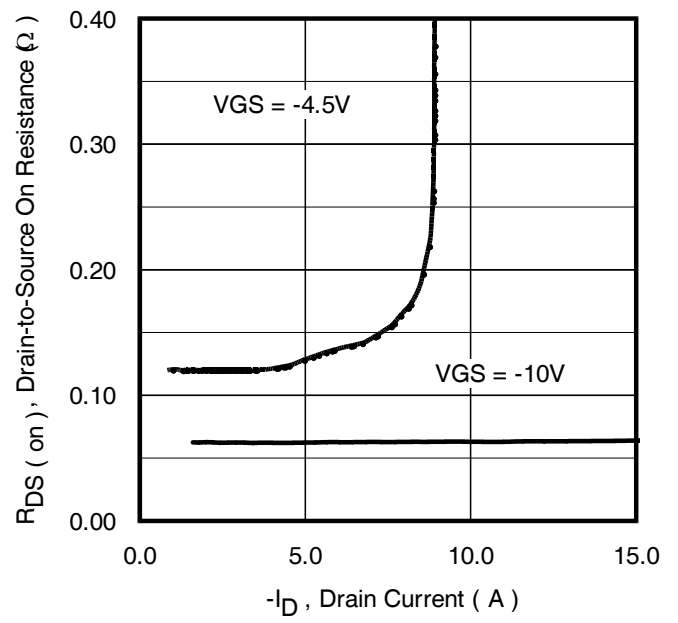


**Fig 8.** Maximum Safe Operating Area

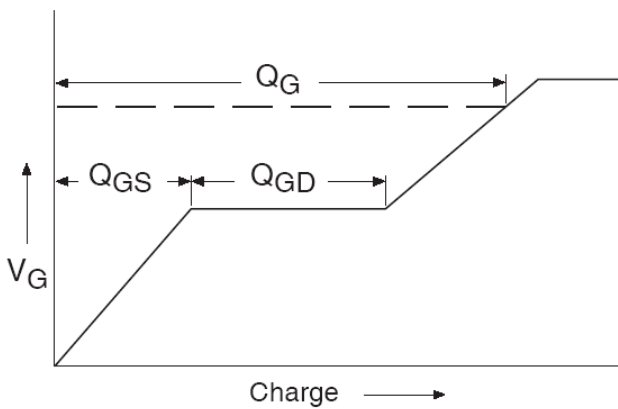

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10a.** Switching Time Test Circuit

**Fig 10b.** Switching Time Waveforms

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



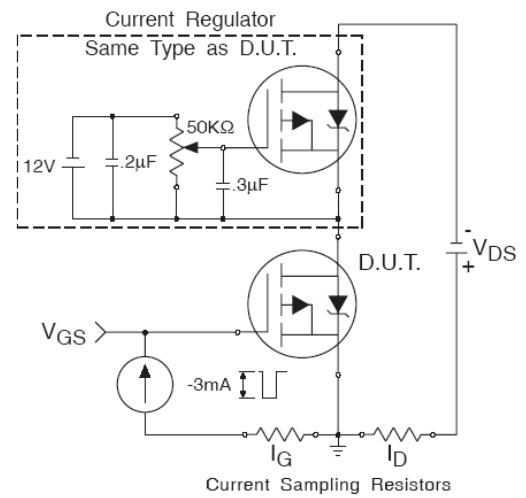
**Fig 12.** Typical On-Resistance Vs. Gate Voltage



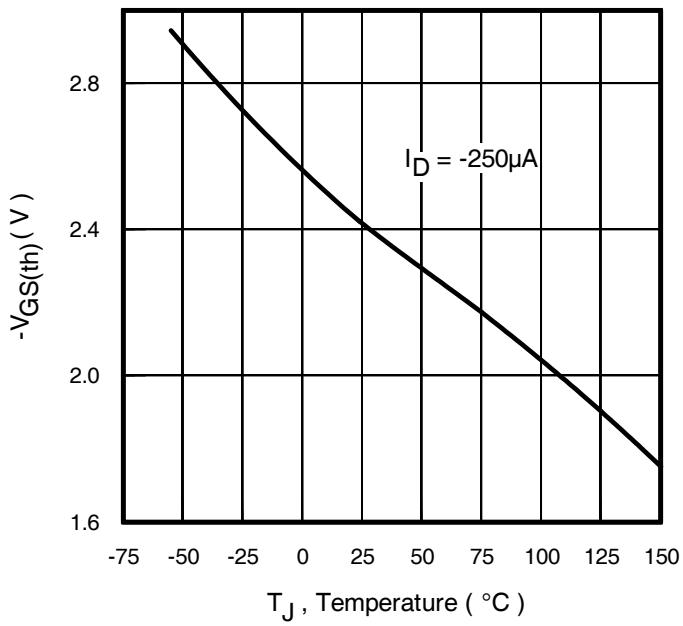
**Fig 13.** Typical On-Resistance Vs. Drain Current



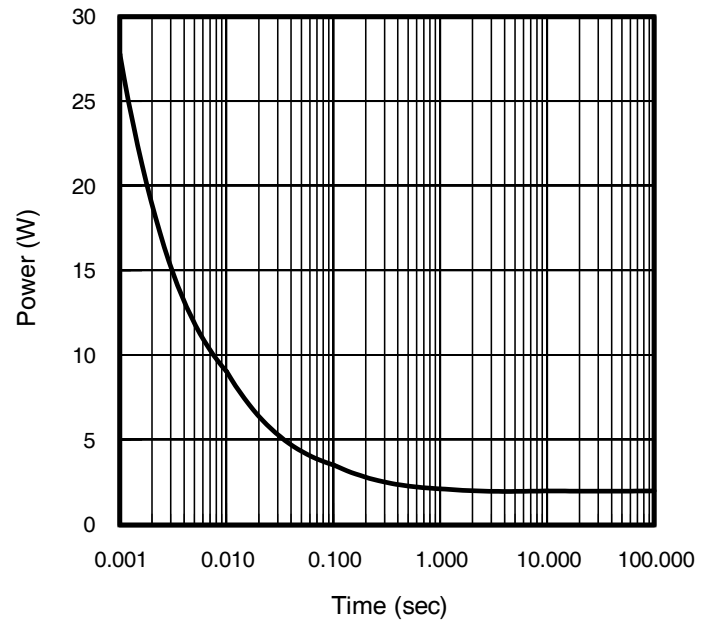
**Fig 14a.** Basic Gate Charge Waveform



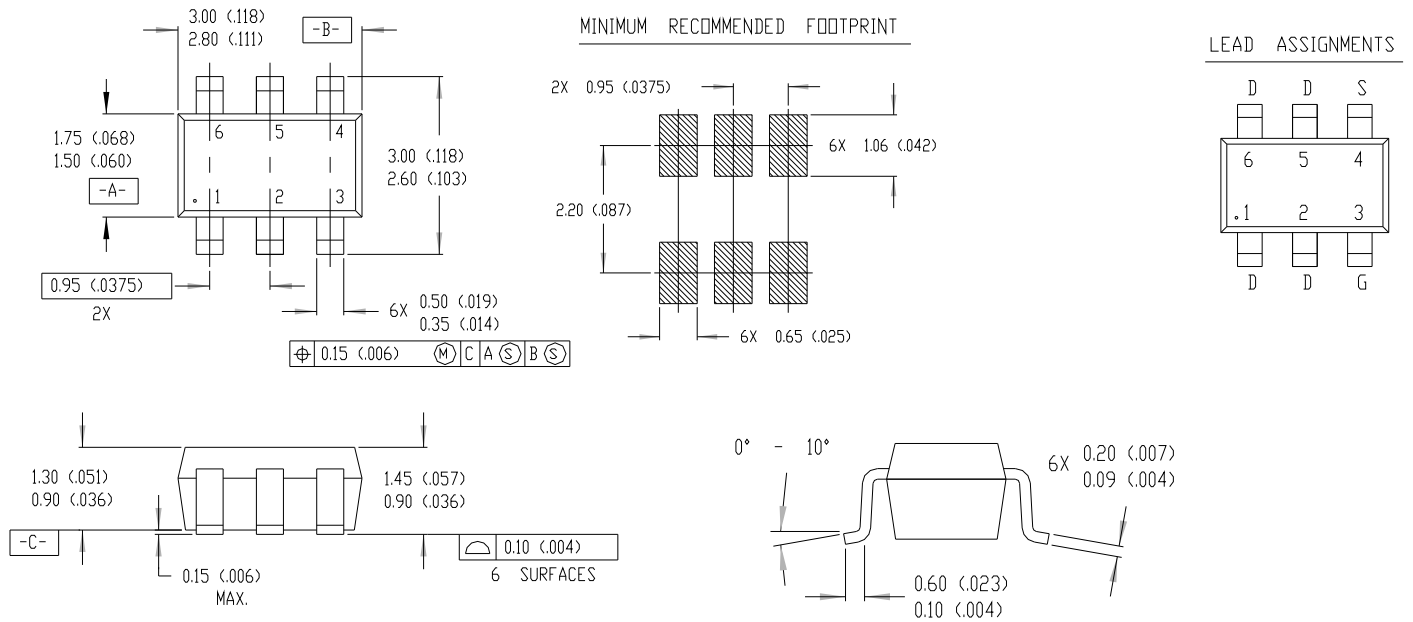
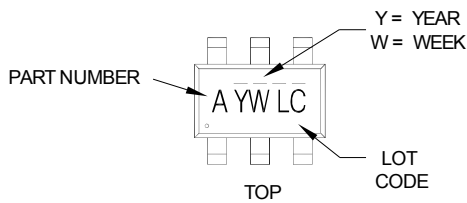
**Fig 14b.** Gate Charge Test Circuit



**Fig 15.** Typical Threshold Voltage Vs. Junction Temperature



**Fig 16.** Typical Power Vs. Time

**TSOP-6 Package Outline**

**TSOP-6 Part Marking Information**

**PART NUMBER CODE REFERENCE:**

- |              |                    |
|--------------|--------------------|
| A = SI3443DV | O = IRLTS6342TRPBF |
| B = IRF5800  | P = IRF58342TRPBF  |
| C = IRF5850  | R = IRF589342TRPBF |
| D = IRF5851  | S = Not applicable |
| E = IRF5852  | T = IRLTS2242TRPBF |
| F = IRF5801  |                    |
| G = IRF5803  |                    |
| H = IRF5804  |                    |
| I = IRF5805  |                    |
| J = IRF5806  |                    |
| K = IRF5810  |                    |
| N = IRF5802  |                    |

Note: A line above the work week (as shown here) indicates Lead-Free.

**DATE CODE MARKING INSTRUCTIONS**

WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

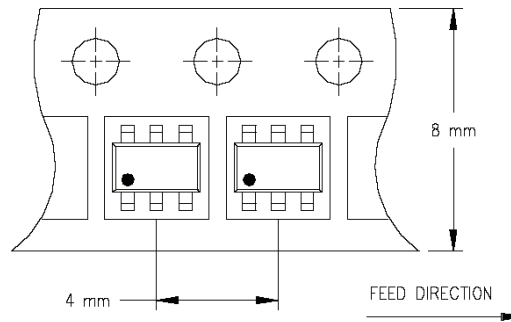
YEAR	Y	WORK WEEK	W	
2011	2001	1	01	A
2012	2002	2	02	B
2013	2003	3	03	C
2014	2004	4	04	D
2015	2005	5		
2016	2006	6		
2017	2007	7		
2018	2008	8		
2019	2009	9		
2020	2010	0	24	X
			25	Y
			26	Z

WW = (27-52) IF PRECEDED BY A LETTER

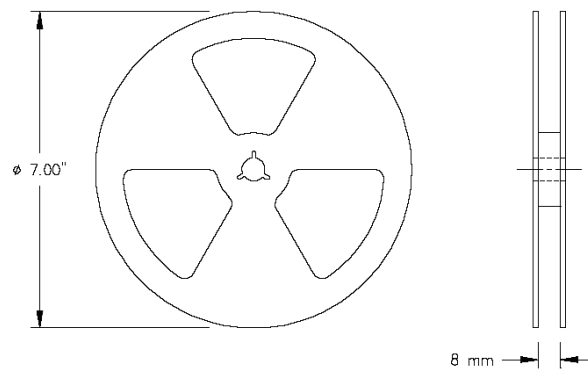
YEAR	Y	WORK WEEK	W	
2011	2001	A	27	A
2012	2002	B	28	B
2013	2003	C	29	C
2014	2004	D	30	D
2015	2005	E		
2016	2006	F		
2017	2007	G		
2018	2008	H		
2019	2009	J		
2020	2010	K	50	X
			51	Y
			52	Z

Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)



**TSOP-6 Tape & Reel Information**

**NOTES:**

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES:**

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**Qualification Information**

<b>Qualification Level</b>	Consumer (per JEDEC JESD47F) †	
<b>Moisture Sensitivity Level</b>	TSOP-6	MSL1 (per JEDEC J-STD-020D) †
<b>RoHS Compliant</b>	Yes	

† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
01/27/2017	<ul style="list-style-type: none"> <li>Changed datasheet with Infineon logo-all pages</li> <li>Updated package outline and part marking on page 8.</li> <li>Added disclaimer on last page.</li> </ul>

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**Document reference**  
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